CMOS ANALOG IC DESIGN

(R22D6803)

DIGITAL NOTES

M.TECH
(I YEAR – I SEM)
(2023-24)

Department of Electronics and Communication Engineering

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

Recognized under 2(f) and 12 (B) of UGC ACT 1956

(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)

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ELECTIVE-I
CMOS ANALOG IC DESIGN

Course Objectives:

- To provide in-depth understanding of different types of MOS devices and modeling techniques
- To understand and design the operation of current mirror circuits
- To demonstrate the analysis and design of amplifiers using CMOS
- To design a various stages of Operational amplifiers using CMOS devices.
- Design and construct the open loop and discrete time comparators using op-amp.

UNIT –I

MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOSDevice Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model forthe MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Currentmirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current andVoltage References, Band gap Reference.

UNIT –III

CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT –IV

CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAmp.

UNIT –V
Comparators
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li

Course Outcomes:

- Model various components in CMOS process to estimate their performance in circuits.
- Analyze and design of MOS and different current mirror circuits including Wilson, cascode current mirror.
- Design of CMOS Amplifiers including Differential, Cascode and high gain amplifier architectures.
- Design of CMOS Operational amplifiers and to measure the characteristics of cascode operational-amplifier.
- Apply and analyze the performance of open loop and discrete time capacitor circuits

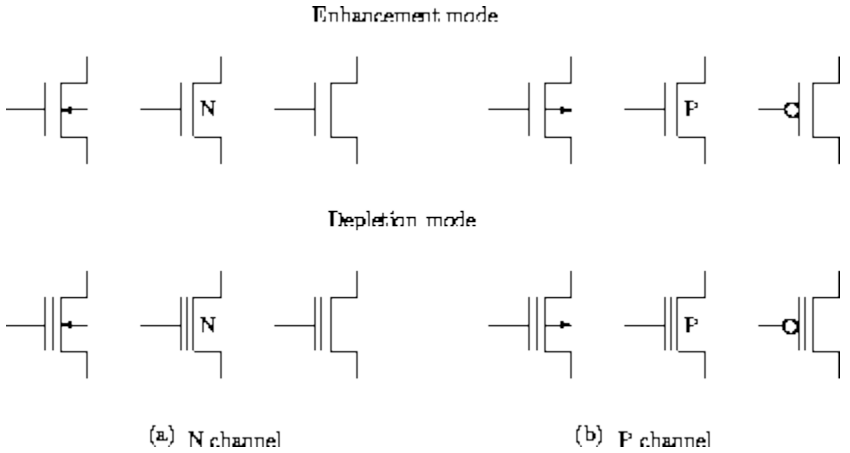
UNIT -I
MOS Devices and Modeling

MOS Transistor:

A **MOS** transistor is primarily a switch for digital devices. Ideally, it works as follows:

If the voltage at the **gate electrode** is "on" , the transistor is "on", too, and current flow between the **source** and **drain** electrodes is possible (almost) without losses.

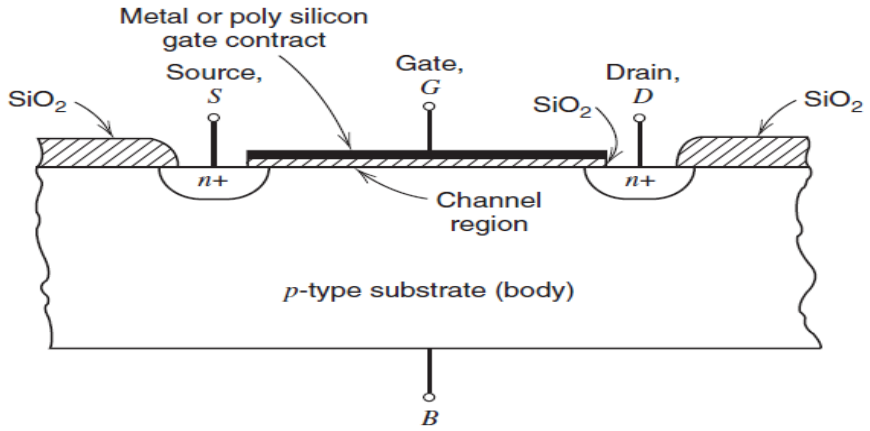
If the voltage at the gate electrode is "off", the transistor is "off", too, and no current flows between the source and drain electrode.



The most basic element in the design of a large scale integrated circuit is the transistor. For the processes this type of transistor available is the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). These transistors are formed as a ``sandwich" consisting of a semiconductor layer, usually a slice, or wafer, from a single crystal of silicon; a layer of silicon dioxide (the oxide) and a layer of metal. These layers are patterned in a manner which permits transistors to be formed in the semiconductor material (the ``substrate"); a diagram showing a typical (idealized) MOSFET is shown in Figure ❑. Silicon dioxide is a very good insulator, so a very thin layer, typically only a few hundred molecules thick, is required. Actually, the transistors which we will use do not use metal for their gate regions, but instead use polycrystalline silicon (poly). Polysilicon gate FET's have replaced virtually all of the older devices using metal gates in large scale integrated circuits. (Both metal and polysilicon FET's are sometimes referred to as IGFET's --- insulated gate field effect transistors, since the silicon dioxide under the gate is an insulator. We will still continue to use the term MOSFET to refer to polysilicon gate FET's.)

Transfer Characteristics of MOS Devices:

A cross section of a typical enhancement-mode *n*-channel MOS (NMOS) transistor is shown in Fig.



Heavily doped *n*-type source and drain regions are fabricated in a *p*-type substrate (often called the body).A thin layer of silicon dioxide is grown over the substrate material and a conductive gate material (metal or polycrystalline silicon) covers the oxide between source and drain. Note that the gate is horizontal in Fig., and we will use this orientation in all descriptions of the physical operation of MOS devices. In operation, the gate-source voltage modifies the conductance of the region under the gate, allowing the gate voltage to control the current flowing between the source and drain. This control can be used to provide gain in analog circuits and switching characteristics in digital circuits.

TRANSISTOR OPERATING POLARTIES

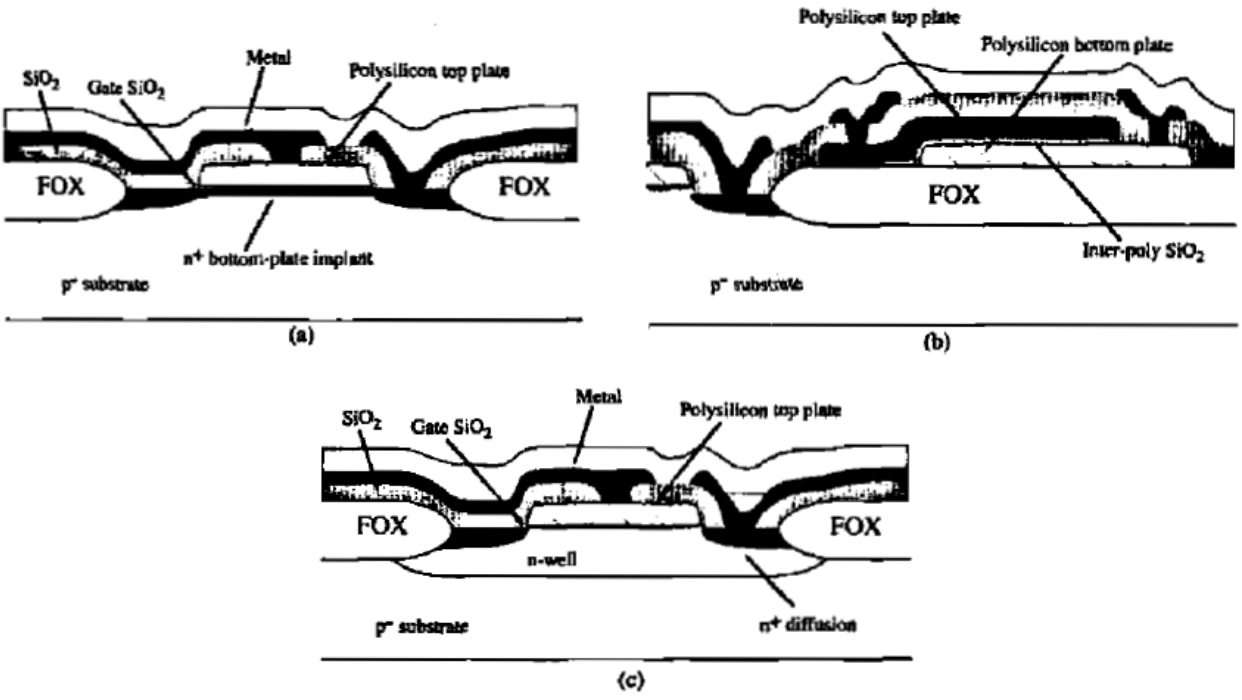
Type of Device	Polarity of v_{GS} and V_T	Polarity of v_{DS}	Polarity of v_{BULK}
n-channel, enhancement	+	+	Most negative
n-channel, depletion	-	+	Most negative
p-channel, enhancement	-	-	Most positive
p-channel, depletion	+	-	Most positive

Passive Components- Capacitor & Resistor:

Capacitors

A good capacitor is often required when designing analog integrated circuits. They are used as compensation capacitors in amplifier designs, gain-determining components in charge amplifiers, bandwidth-determining components in gm/C filters, charge storage devices in switched-capacitor filters and digital-to-analog converters, and other places as well. The desired characteristics for capacitors used in these applications are:

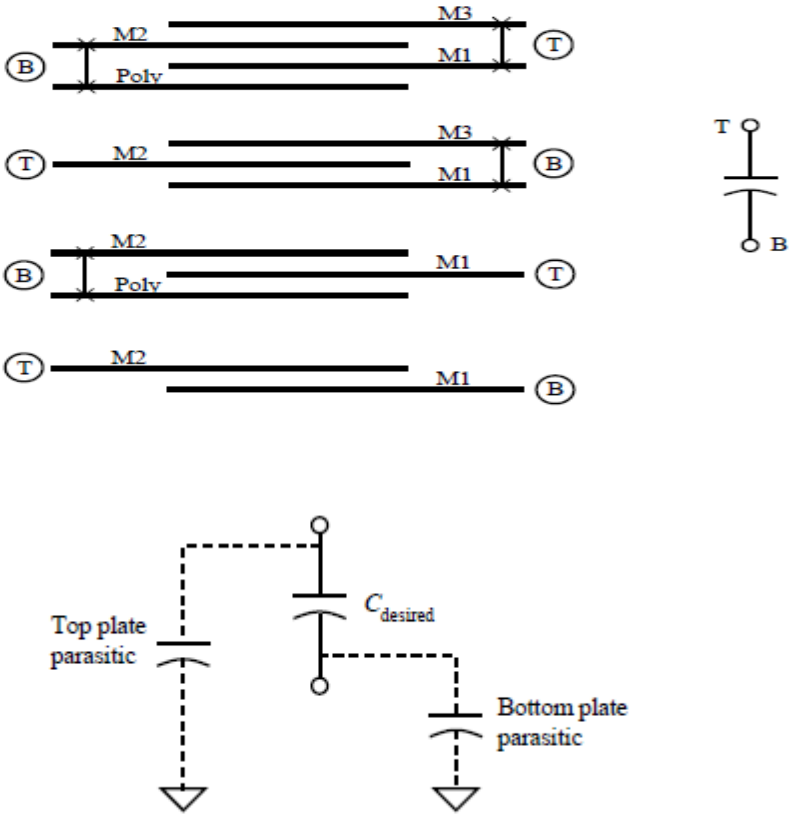
- Good matching accuracy
- Low voltage coefficient
- High ratio of desired capacitance to parasitic capacitance
- High capacitance per unit area
- Low temperature dependence



MOS capacitors. (a) Polysilicon–oxide channel. (b) Polysilicon–oxide–polysilicon. (c) Accumulation MOS capacitor.

Component Type	Range of Values	Matching Accuracy	Temperature Coefficient	Voltage Coefficient
MOS capacitor	2.2–2.7 fF/μm^2	0.05%	50 ppm/°C	50 ppm/V
Poly/poly capacitor	0.8–1.0 fF/μm^2	0.05%	50 ppm/°C	50 ppm/V
M1–Poly capacitor	0.021–0.025 fF/μm^2	1.5%	—	—
M2–M1 capacitor	0.021–0.025 fF/μm^2	1.5%	—	—
M3–M2 capacitor	0.021–0.025 fF/μm^2	1.5%	—	—
p^+ Diffused resistor	80–150 Ω/□	0.4%	1500 ppm/°C	200 ppm/V
n^+ Diffused resistor	50–80 Ω/□	0.4%	1500 ppm/°C	200 ppm/V
Poly resistor	20–40 Ω/□	0.4%	1500 ppm/°C	100 ppm/V
n-Well resistor	1–2 kΩ/□	—	8000 ppm/°C	10k ppm/V

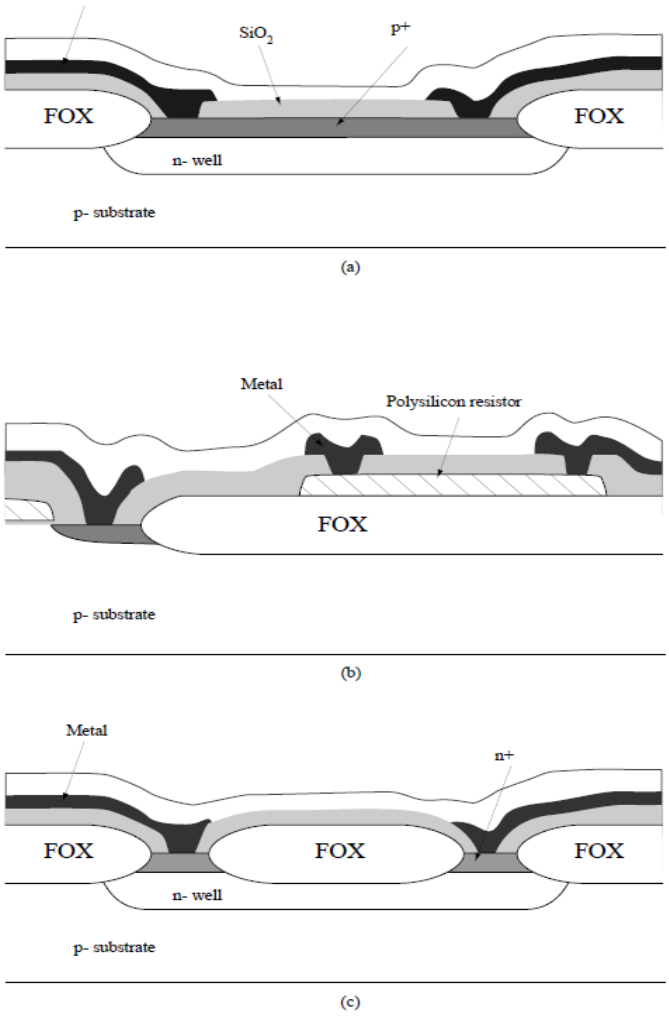
Metal-Metal and Metal-Metal-Poly Capacitors



A model for the integrated capacitors showing top and bottom plate parasitics.

Resistors

The other passive component compatible with MOS technology is the resistor. Even though we shall use circuits consisting of primarily MOS active devices and capacitors, some applications, such as digital-to-analog conversion, use the resistor. Resistors compatible with the MOS technology of this section include diffused, polysilicon, and n-well (or p-well) resistors. Though not as common, metal can be used as a resistor as well.



Resistors. (a) Diffused (b) Polysilicon (c) N-well

PASSIVE COMPONENT SUMMARY

(0.8μm Technology)

Component Type	Range of Values	Matching Accuracy	Temperature Coefficient	Voltage Coefficient	Absolute Accuracy
Poly/poly capacitor	0.8-1.0 fF/μm^2	0.05%	50 ppm/°C	50ppm/V	±10%
MOS capacitor	2.2-2.5 fF/μm^2	0.05%	50 ppm/°C	50ppm/V	±10%
MOM capacitor	0.02-0.03 fF/μm^2	1.5%			±10%
Diffused resistor	20-150 Ω/sq.	0.4%	1500 ppm/°C	200ppm/V	±35%
Polysilicide R	2-15 Ω/sq.				
Poly resistor	20-40 Ω/sq.	0.4%	1500 ppm/°C	100ppm/V	±30%
N-well resistor	1-2k Ω/sq.	0.4%	8000 ppm/°C	10k ppm/V	±40%

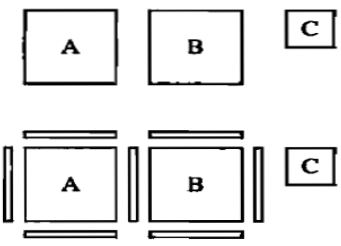
Integrated circuit Layout:

A unique aspect of integrated-circuit design is that it requires understanding of the circuit beyond the schematic. A circuit defined and functioning properly at the schematic level can fail if it is not correctly designed physically. Physical design, in the context of integrated circuits, is referred to as *layout*.

Matching Concepts

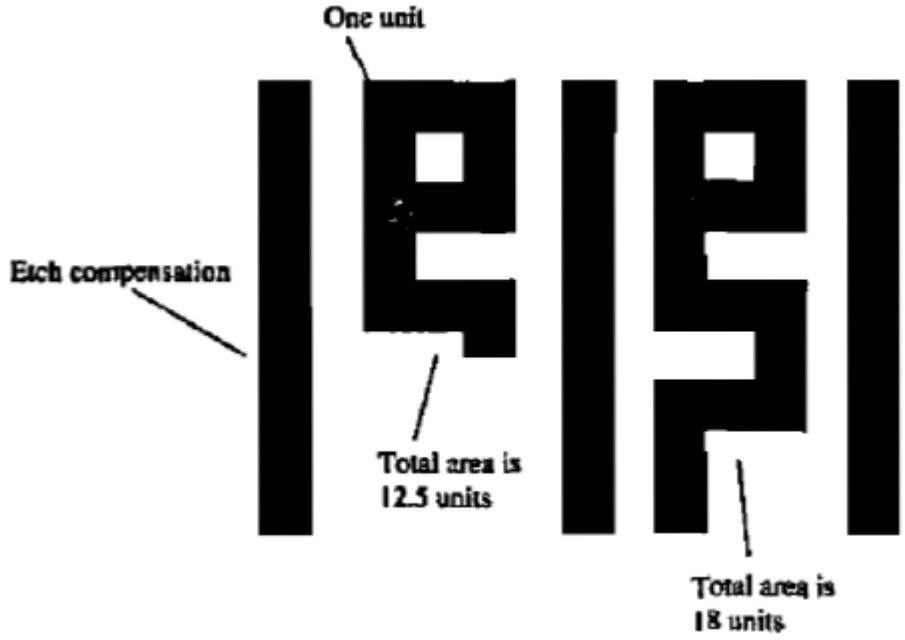
As will be seen in later chapters, matching the performance of two or more components is very important to overall circuit operation. Since matching is dependent on layout topology, it is appropriate to discuss it here.

The rule for making two components electrically equivalent is simply to draw them as identical units. This is the *unit-matching* principle. To say that two components are identical means that both they and their surroundings must be identical. This concept can be explained in nonelectrical terms.



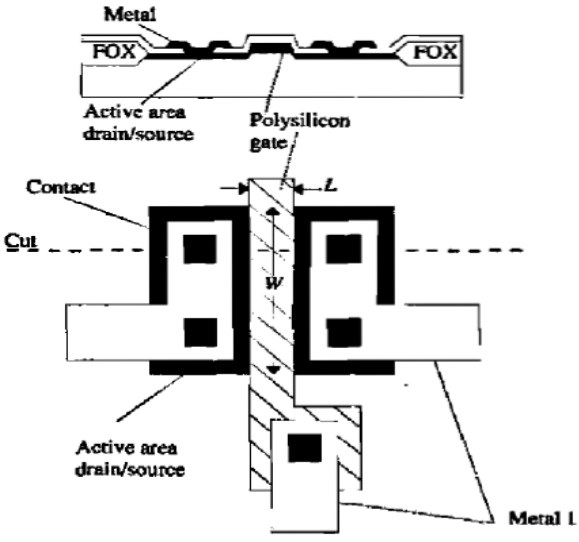
MOS Transistor Layout

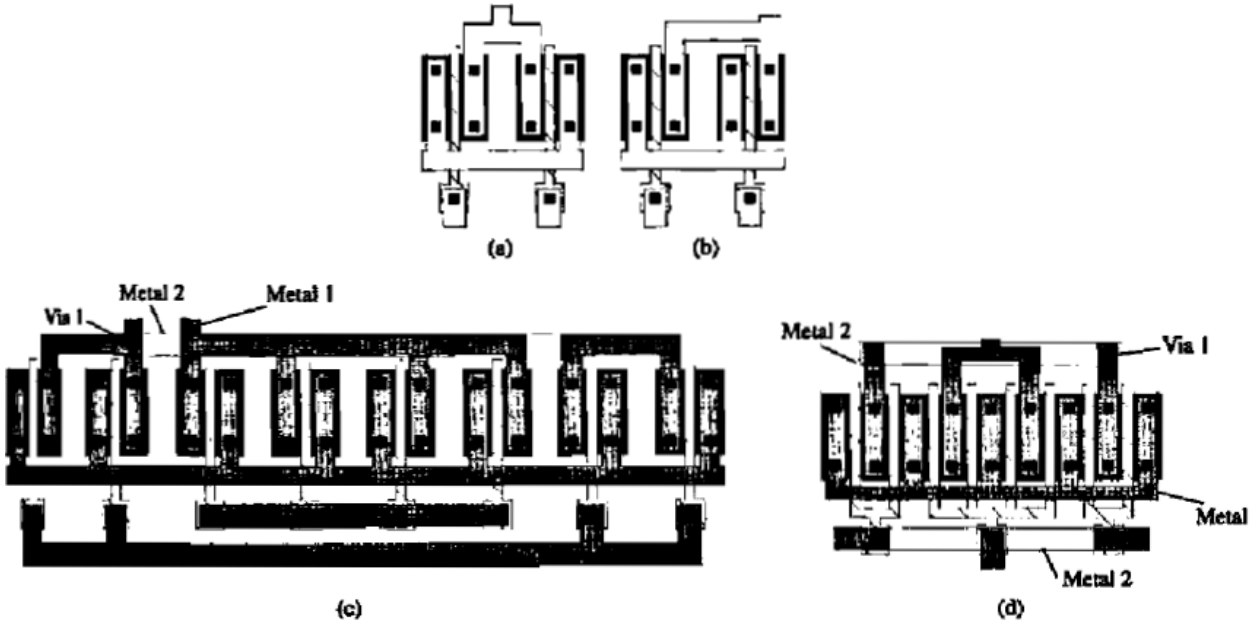
Transistors that are used for analog applications are drawn as linear *stripes* as opposed to a transistor drawn with a bend in the gate. The dimensions that will be important later on are the width and length of the transistor as well as the area and periphery of the drain and source. It is the *W/L* ratio that is the dominant dimensional component governing transistor conduction, and the area and periphery of the drain and source that determine drain and source capacitance on a per-device basis.



Y path technique

Resistor Layout





Example layout of MOS transistors using (a) mirror symmetry, (b) photolithographic invariance, and (c) two transistors sharing a common source and laid out to achieve both photolithographic invariance and common centroid. (d) Compact layout of (c).

$$R = \frac{\rho L}{WT} \quad (\Omega)$$

RESISTANCE CALCULATION

Given a polysilicon resistor like that drawn in Fig. 2.6-8(a) with $W = 0.8\ \mu m$ and $L = 20\ \mu m$, calculate ρ_s (in $\Omega/\square$), the number of squares of resistance, and the resistance value. Assume that ρ for polysilicon is $9 \times 10^{-4}\ \Omega$-cm and the polysilicon is 3000 Å thick. Ignore any contact resistance.

Solution

First calculate ρ_s.

$$\rho_s = \frac{\rho}{T} = \frac{9 \times 10^{-4}\ \Omega\,\text{cm}}{3000 \times 10^{-8}\ \text{cm}} = 30\ \Omega/\square$$

The number of squares of resistance, N, is

$$N = \frac{L}{W} = \frac{20\ \mu m}{0.8\ \mu m} = 25$$

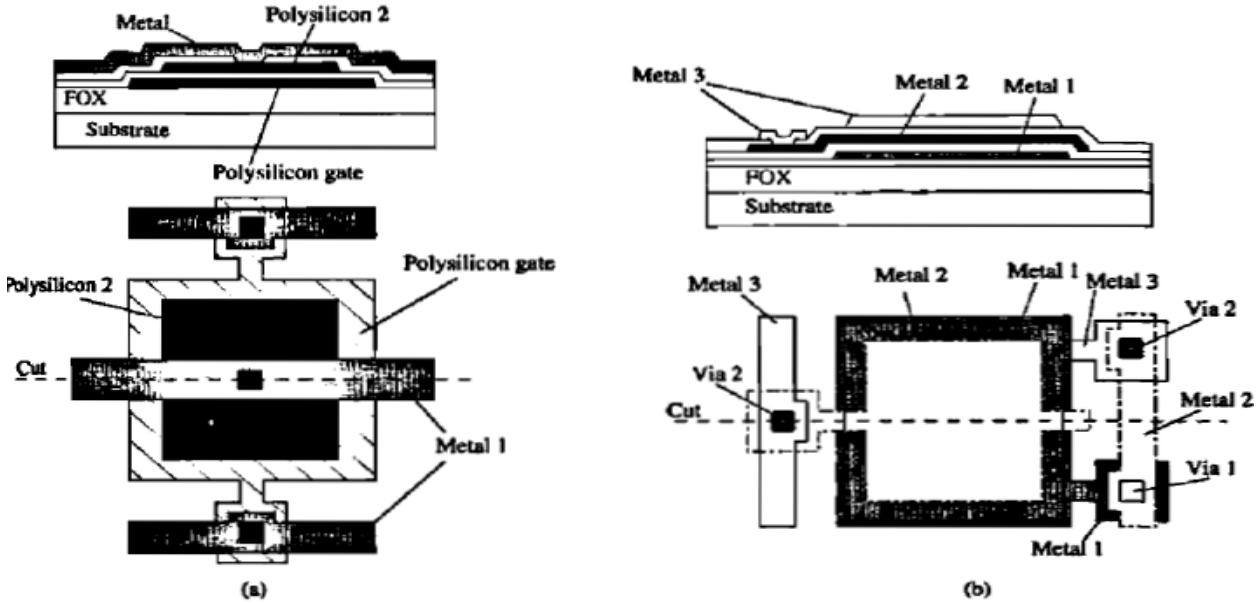
giving the total resistance as

$$R = \rho_s \times N - 30 \times 25 = 750\ \Omega$$

Capacitor Layout

Capacitors can be constructed in a variety of ways depending on the process as well as the particular application. Only two detailed capacitor layouts will be shown here.
The double-polysilicon capacitor layout is illustrated in Fig.

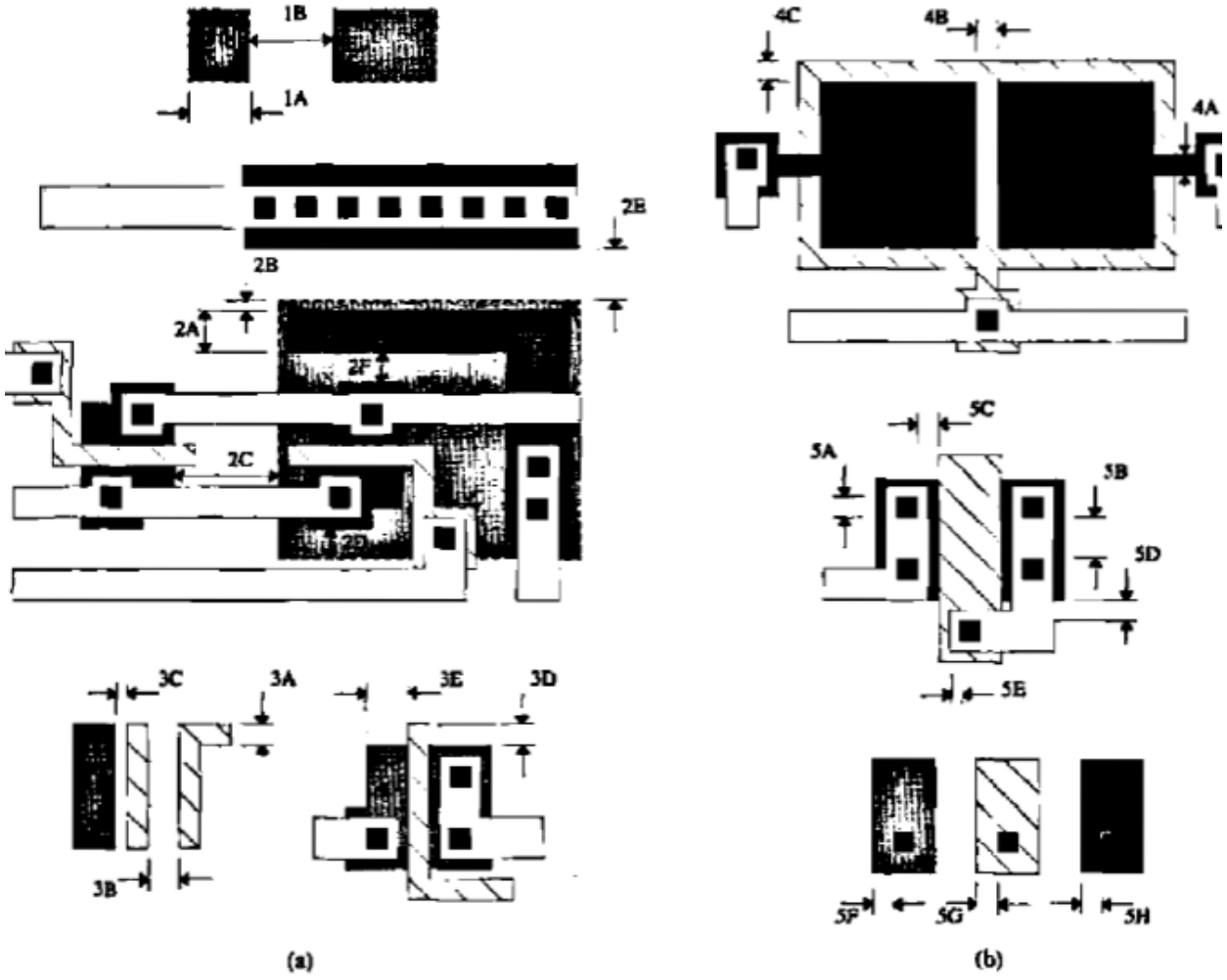
$$C = \frac{\varepsilon_{ox} A}{t_{ox}} = C_{ox} A$$



Example layout (a) double-polysilicon capacitor and (b) triple-level metal capacitor

Layout Rules

As the layout of an integrated circuit is being drawn, there are *layout rules* that must be observed in order to ensure that the integrated circuit is manufacturable. Layout rules governing manufacturability arise, in part, from the fact that at each mask step in the process, features of the next photomask must be aligned to features previously defined on the integrated circuit. Even when using precision automatic alignment tools, there is still some error in alignment. In some cases, alignment of two layers is critical to circuit operation. As a result, alignment tolerances impose a limitation of feature size and orientation with respect to other layers on the circuit.



Design Rules for a Double-Metal, Double-Polysilicon, N-Well, Bulk CMOS Process.

Minimum Dimension Resolution (λ)

1. N-Well
   - 1A. width 6
   - 1B. spacing 12
2. Active Area (AA)
   - 2A. width 4

   Spacing to Well
   - 2B. AA-n contained in n-Well 1
   - 2C. AA-n external to n-Well 10
   - 2D. AA-p contained in n-Well 3
   - 2E. AA-p external to n-Well 4

   Spacing to other AA (inside or outside well)
   - 2F. AA to AA (p or n) 3

3. Polysilicon Gate (Capacitor bottom plate)

3A. width.....2

3B. spacing 3

3C. spacing of polysilicon to AA (over field).....1

3D. extension of gate beyond AA (transistor width dir.) 2

3E. spacing of gate to edge of AA (transistor length dir.) 4

4. Polysilicon Capacitor top plate

4A. width.....2

4B. spacing 2

4C. spacing to inside of polysilicon gate (bottom plate).....2

5. Contacts

5A. size 2x2

5B. spacing 4

5C. spacing to polysilicon gate 2

5D. spacing polysilicon contact to AA 2

5E. metal overlap of contact 1

5F. AA overlap of contact 2

5G. polysilicon overlap of contact.....2

5H. capacitor top plate overlap of contact.....2

6. Metal-1

6A. width.....3

6B. spacing 3

7. Via

7A. size 3x3

7B. spacing 4

7C. enclosure by Metal-1 1

7D. enclosure by Metal-2 1

8. Metal-2

8A. width 4

8B. spacing 3

Bonding Pad

8C. spacing to AA 24

8D. spacing to metal circuitry 24

8E. spacing to polysilicon gate 24

9. Passivation Opening (Pad)

9A. bonding-pad opening ..... 100μm x 100μm

9B. bonding-pad opening enclosed by Metal-2 8

9C. bonding-pad opening to pad opening space 40

CMOS Device Modeling:

Before one can design a circuit to be integrated in CMOS technology, one must first have a model describing the behavior of all the components available for use in the design. A model can take the form of mathematical equations, circuit representations, or tables. Most of the modeling used in this text will focus on the active and passive devices discussed in the previous chapter as opposed to higher-level modeling such as macromodeling or behavioral modeling.

SPICE was originally implemented in FORTRAN where all input was required to be uppercase ASCII characters. Lowercase, greek, and super/subscripting were not allowed. Modern SPICE implementations generally accept (but do not distinguish between) uppercase and lowercase but the tradition of using uppercase ASCII still lives on. This is particularly evident in the device model parameters. Since greek characters are not available, these were simply spelled out, for example, γ entered as GAMMA. Superscripts and subscripts were simply not used.

Simple MOS Large-Signal Model:

The large signal model is nonlinear and is used to solve for the dc values of the device currents given the device voltages.

The large signal models for SPICE:

Basic drain current models -

1. Level 1 - Shichman-Hodges (V_T, K', γ, λ, ϕ, and N_{SUB})
2. Level 2 - Geometry-based analytical model. Takes into account second-order effects (varying channel charge, short-channel, weak inversion, varying surface mobility, etc.)
3. Level 3 - Semi-empirical short-channel model
4. Level 4 - BSIM model. Based on automatically generated parameters from a process characterization. Good weak-strong inversion transition.

Basic model auxilliary parameters include capacitance [Meyer and Ward-Dutton (charge-conservative)], bulk resistances, depletion regions, etc..

Small Signal Model

Based on the linearization of any of the above large signal models.

Simulator Software

SPICE2 - Generic SPICE available from UC Berkeley (FORTRAN)

SPICE3 - Generic SPICE available from UC Berkeley (C)

SPICE- Every other SPICE simulator!

All large-signal models will be developed for the n-channel MOS device with the positive polarities of voltages and currents shown in Fig. 3.1-1(a). The same models can be used for the p-channel MOS device if all voltages and currents are multiplied by -1 and the absolute value of the p-channel threshold is used. This is equivalent to using the voltages and currents defined by Fig. 3.1-1(b), which are all positive quantities. As mentioned in Chapter 1, lowercase variables with capital subscripts will be used for the variables of large-signal models and lowercase variables with lowercase subscripts will be used for the variables of small-signal models. When the voltage or current is a model parameter, such as threshold voltage, it will be designated by an uppercase variable and an uppercase subscript.

When the length and width of the MOS device is greater than about 10 μm, the substrate doping is low, and when a simple model is desired, the model suggested by Sah [3] and used in SPICE by Shichman and Hodges [4] is very appropriate. This model was developed in Eq. (2.3-27) and is given below.

$$i_D = \frac{\mu_0 C_{ox} W}{L}\left[(v_{GS} - V_T) - \left(\frac{v_{DS}}{2}\right)\right]v_{DS} \tag{3.1-1}$$

The terminal voltages and currents have been defined in the previous chapter. The various parameters of Eq. (3.1-1) are defined as

μ_0 = surface mobility of the channel for the n-channel or p-channel device (cm^2/V-s)

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ = capacitance per unit area of the gate oxide (F/cm^2)

W = effective channel width

L = effective channel length

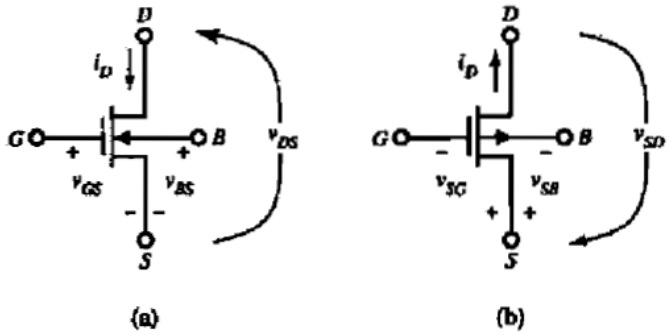


Figure 3.1-1 Positive sign convention for (a) n-channel and (b) p-channel MOS transistor.

The threshold voltage V_T is given by Eq. (2.3-19) for an n-channel transistor:

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right)$$

$$V_{T0} = V_T(v_{SB} = 0) = V_{FB} + 2|\phi_F| + \frac{\sqrt{2q\varepsilon_{Si}N_{SUB}2|\phi_F|}}{C_{ox}}$$

$$\gamma = \text{bulk threshold parameter } (V^{1/2}) = \frac{\sqrt{2\varepsilon_{Si}qN_{SUB}}}{C_{ox}}$$

$$\phi_F = \text{strong inversion surface potential (V)} = \frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right)$$

$$V_{FB} = \text{flatband voltage (V)} = \phi_{MS} - \frac{Q_{ss}}{C_{ox}}$$

$$\phi_{MS} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) \quad [\text{Eq. (2.3-17)}]$$

$$\phi_F(\text{substrate}) = \frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right)[\text{n-channel with p-substrate}]$$

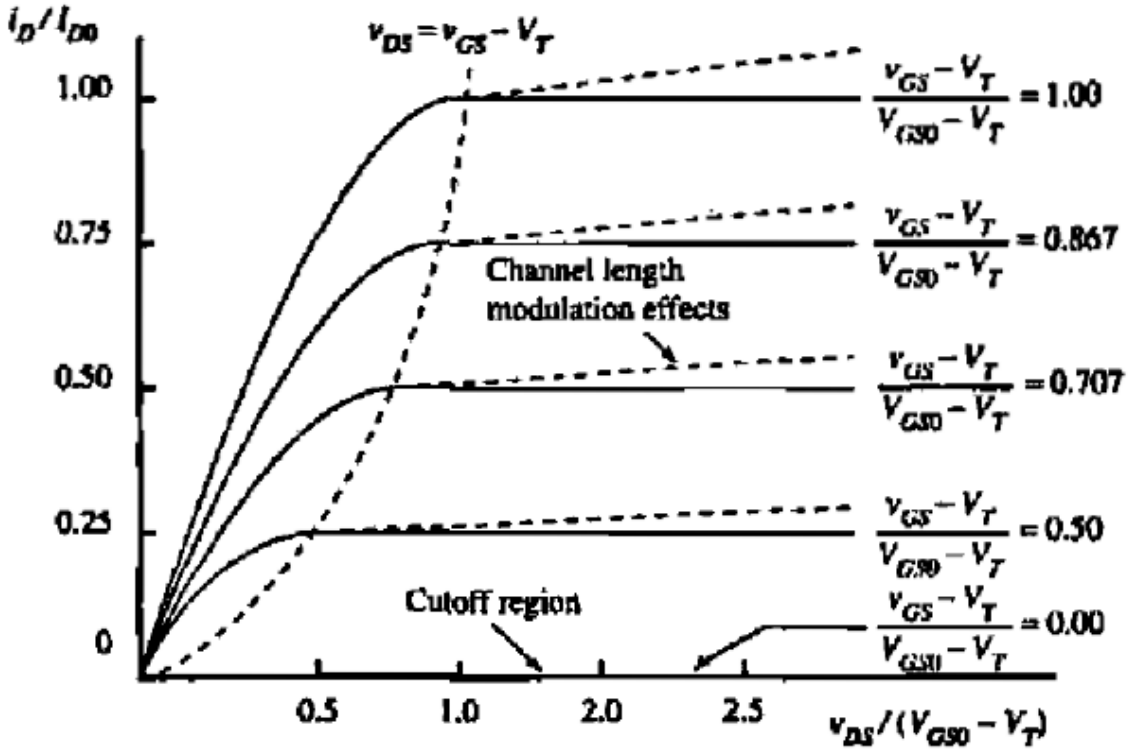
$$\phi_F(\text{gate}) = \frac{kT}{q}\ln\left(\frac{N_{GATE}}{n_i}\right)[\text{n-channel with } n^+ \text{ polysilicon gate}]$$

$$Q_{ss} = \text{oxide-charge} = qN_{ss}$$

k = Boltzmann's constant

T = temperature (K)

n_i = intrinsic carrier concentration



Output characteristics of the MOS device.

APPLICATION OF THE SIMPLE MOS LARGE-SIGNAL MODEL

Assume that the transistors in Fig. 3.1-1 have a W/L ratio of 5 μm/1 μm and that the large-signal model parameters are those given in Table 3.1-2. If the drain, gate, source, and bulk voltages of the n-channel transistor are 3 V, 2 V, 0 V, and 0 V, respectively, find the drain current. Repeat for the p-channel transistor if the drain, gate, source, and bulk voltages are −3 V, −2 V, 0 V, and 0 V, respectively.

Solution

We must first determine in which region the transistor is operating. Equation (3.1-15) gives $v_{DS}(\text{sat})$ as 2 V − 0.7 V = 1.3 V. Since v_{DS} is 3 V, the n-channel transistor is in the saturation region. Using Eq. (3.1-18) and the values from Table 3.1-2, we have

$$i_D = \frac{K_N' W}{2L}(v_{GS} - V_{TN})^2(1 + \lambda_N v_{DS})$$

$$= \frac{110 \times 10^{-6}(5\ \mu\text{m})}{2(1\ \mu\text{m})}(2 - 0.7)^2(1 + 0.04 \times 3) = 520\ \mu\text{A}$$

Evaluation of Eq. (3.1-15) for the p-channel transistor is given as

$$v_{SD}(\text{sat}) = v_{SG} - |V_{TP}| = 2\ \text{V} - 0.7\ \text{V} = 1.3\ \text{V}$$

Since v_{SD} is 3 V, the p-channel transistor is also in the saturation region, and Eq. (3.1-17) is applicable. The drain current of Fig. 3.1-1(b) can be found using the values from Table 3.1-2 as

$$i_D = \frac{K_p' W}{2L}(v_{SG} - |V_{TP}|)^2 (1 + \lambda_p v_{SD})$$

$$= \frac{50 \times 10^{-6}(5\ \mu\text{m})}{2(1\ \mu\text{m})}(2 - 0.7)^2(1 + 0.05 \times 3) = 243\ \mu\text{A}$$

It is often useful to describe v_{GS} in terms of i_D in saturation as shown below:

$$v_{GS} = V_T + \sqrt{2i_D/\beta} \tag{3.1-19}$$

This expression illustrates that there are two components to v_{GS}—an amount to invert the channel plus an additional amount to support the desired drain current. This second component is often referred to in the literature as V_{ON}. Thus V_{ON} can be defined as

$$V_{ON} = \sqrt{2i_D/\beta} \tag{3.1-20}$$

The term V_{ON} should be recognized as the term for saturation voltage V_{DS} (sat). They can be used interchangeably.

Other Model Parameters:

The large-signal model also includes several other characteristics such as the source/drain bulk junctions, source/drain ohmic resistances, various capacitors, and noise. The complete version of the large-signal model is given in Fig. 3.2-1.

The diodes of Fig. 3.2-1 represent the pn junctions between the source and substrate and the drain and substrate. For proper transistor operation, these diodes must always be reverse biased. Their purpose in the dc model is primarily to model leakage currents. These currents are expressed as

$$i_{BD} = I_s\left[\exp\left(\frac{qv_{BD}}{kT}\right) - 1\right]$$

and

$$i_{BS} = I_s\left[\exp\left(\frac{qv_{BS}}{kT}\right) - 1\right]$$

where I_s is the reverse saturation current of a pn junction, q is the charge of an electron, k is Boltzmann's constant, and T is temperature in kelvin units.

The resistors r_D and r_S represent the ohmic resistance of the drain and source, respectively. Typically, these resistors may be 50–100 Ω* and can often be ignored at low drain currents.

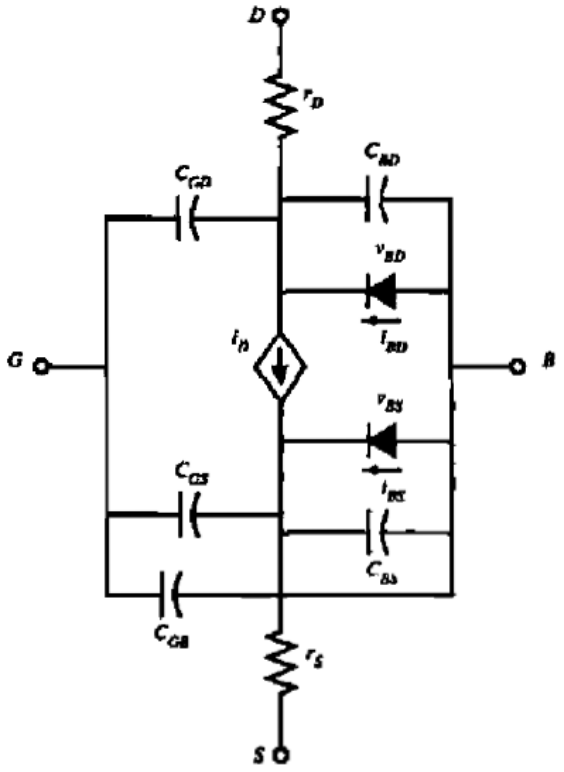


Figure 3.2-1 Complete large-signal model for th MOS transistor.

The capacitors of Fig. 3.2-1 can be separated into three types. The first type includes capacitors C_{BD} and C_{BS}, which are associated with the back-biased depletion region between the drain and substrate and the source and substrate. The second type includes capacitors C_{GD}, C_{GS}, and C_{GB}, which are all common to the gate and are dependent on the operating condition of the transistor. The third type includes parasitic capacitors, which are independent of the operating conditions.

Small-Signal Model for the MOS Transistor

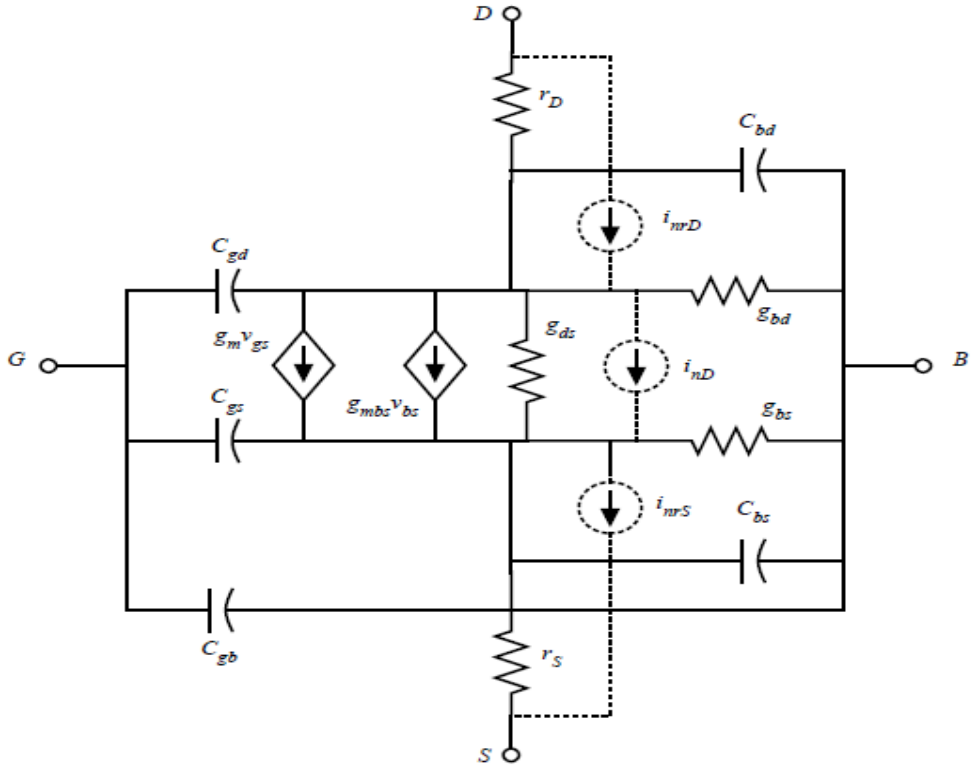


Figure 3.3-1 Small-signal model of the MOS transistor.

$$g_{bd} = \frac{\partial I_{BD}}{\partial V_{BD}} \text{ (at the quiescent point)} \cong 0$$

and

$$g_{bs} = \frac{\partial I_{BS}}{\partial V_{BS}} \text{ (at the quiescent point)} \cong 0$$

The channel conductances, g_m, g_{mbs}, and g_{ds} are defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ (at the quiescent point)}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} \text{ (at the quiescent point)}$$

and

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \text{ (at the quiescent point)}$$

Saturation Region

$$g_m = \sqrt{(2K'W/L)|I_D|(1+\lambda V_{DS})} \cong \sqrt{(2K'W/L)|I_D|}$$

$$g_{mbs} = \frac{-\partial I_D}{\partial V_{SB}} = -\left(\frac{\partial I_D}{\partial V_T}\right)\left(\frac{\partial V_T}{\partial V_{SB}}\right)$$

Noting that $\frac{\partial I_D}{\partial V_T} = \frac{-\partial I_D}{\partial V_{GS}}$, we get

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = \eta\, g_m$$

$$g_{ds} = g_o = \frac{I_D \lambda}{1+\lambda V_{DS}} \cong I_D \lambda$$

Relationships of the Small Signal Model Parameters upon the DC Values of Voltage and Current in the Saturation Region.

Small Signal Model Parameters	DC Current	DC Current and Voltage	DC Voltage
g_m	$\cong (2K' I_D W/L)^{1/2}$	–	$\cong \frac{2K' W}{L}(V_{GS} - V_T)$
g_{mbs}	—	$\frac{\gamma (2I_D\beta)^{1/2}}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$	$\frac{\gamma(\beta(V_{GS}-V_T))}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$
g_{ds}	$\cong \lambda I_D$	—	—

Nonsaturation region

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = \beta V_{DS}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\beta\gamma V_{DS}}{2(2|\phi_F| + V_{SB})^{1/2}}$$

and

$$g_{ds} = \beta(V_{GS} - V_T - V_{DS})$$

Relationships of the Small-Signal Model Parameters upon the DC Values of Voltage and Current in the Nonsaturation Region.

Small Signal Model Parameters	DC Voltage and/or Current Dependence
g_m	$= \beta V_{DS}$
g_{mbs}	$\frac{\beta\gamma V_{DS}}{2(2\|\phi_F\| + V_{SB})^{1/2}}$
g_{ds}	$= \beta(V_{GS} - V_T - V_{DS})$

Noise

$$\overline{i}^2_{nrD} = \left(\frac{4kT}{r_D}\right)\Delta f \quad (A^2)$$

$$\overline{i}^2_{nrS} = \left(\frac{4kT}{r_S}\right)\Delta f \quad (A^2)$$

and

$$\overline{i}^2_{nD} = \left[\frac{8kT\, g_m(1+\eta)}{3} + \frac{(KF)I_D}{f C_{ox} L^2}\right]\Delta f \quad (A^2)$$

Computer Simulation Models:

The large-signal model of the MOS device previously discussed is simple to use for hand calculations but neglects many important second-order effects. While a simple model for hand calculation and design intuition is critical, a more accurate model is required for computer simulation. There are many model choices available for the designer when choosing a device model to use for computer simulation. At one time, HSPICE* supported 43 different MOSFET models [2] (many of which were company proprietary) while SmartSpice publishes support for 14 [9]. Which model is the right one to use? In the fabless semiconductor environment, the user must use the model provided by the wafer foundry. In companies where the foundry is captive (i.e., the company owns its own wafer fabrication facility) a modeling group provides the model to circuit designers. It is seldom that a designer chooses a model and performs parameter extraction to get the terms for the model chosen.

The SPICE LEVEL 3 dc model will be covered in some detail because it is a relatively straightforward extension of the LEVEL 2 model. The BSIM3v3 model will be introduced but the detailed equations will not be presented because of the volume of equations required to describe it—there are other good texts that deal with the subject of modeling exclusively [10,11], and there is little additional design intuition derived from covering the details.

Models developed for computer simulation have improved over the years but no model has yet been developed that, with a single set of parameters, covers device operation for all possible geometries. Therefore, many SPICE simulators offer a feature called "model binning." Parameters are derived for transistors of different geometry (W's and L's) and the simulator determines which set of parameters to use based on the particular W and L called out in the device instantiation line in the circuit description. The circuit designer need only be aware of this since the binning is done by the model provider.

SPICE Level 3 Model

The large-signal model of the MOS device previously discussed neglects many important second-order effects. Most of these second-order effects are due to narrow or short channel dimensions (less than about 3μm). We shall also consider the effects of temperature upon the parameters of the MOS large signal model.
We first consider second-order effects due to small geometries. When v_{GS} is greater than V_T, the drain current for a small device can be given as

Drain Current

$$i_{DS} = \text{BETA}\left[v_{GS} - V_T - \left(\frac{1+f_b}{2}\right)v_{DE}\right]\cdot v_{DE} \tag{1}$$

$$\text{BETA} = \text{KP}\frac{W_{\text{eff}}}{L_{\text{eff}}} = \mu_{\text{eff}}\text{COX}\frac{W_{\text{eff}}}{L_{\text{eff}}} \tag{2}$$

$$L_{\text{eff}} = L - 2(\text{LD}) \tag{3}$$

$$W_{\text{eff}} = W - 2(\text{WD}) \tag{4}$$

$$v_{DE} = \min(v_{DS}, v_{DS}(\text{sat})) \tag{5}$$

$$f_b = f_n + \frac{\text{GAMMA}\cdot f_s}{4(\text{PHI} + v_{SB})^{1/2}} \tag{6}$$

Note that PHI is the SPICE model term for the quantity $2\phi_f$. Also be aware that PHI is always positive in SPICE regardless of the transistor type (p- or n-channel).

$$f_n = \frac{\text{DELTA}}{W_{\text{eff}}}\frac{\pi\varepsilon_{\text{si}}}{2\cdot\text{COX}} \tag{7}$$

$$f_s = 1 - \frac{x_j}{L_{\text{eff}}}\left\{\frac{\text{LD}+wc}{x_j}\left[1-\left(\frac{wp}{x_j+wp}\right)^2\right]^{1/2} - \frac{\text{LD}}{x_j}\right\} \tag{8}$$

$$wp = xd\,(\text{PHI} + v_{SB})^{1/2} \tag{9}$$

$$xd = \left(\frac{2\cdot\varepsilon_{si}}{q\cdot\text{NSUB}}\right)^{1/2} \tag{10}$$

$$wc = x_j \left[k_1 + k_2 \left(\frac{wp}{x_j} \right) - k_3 \left(\frac{wp}{x_j} \right)^2 \right] \tag{11}$$

$k_1 = 0.0631353$, $k_2 = 0.08013292$, $k_3 = 0.01110777$

Threshold Voltage

$$V_T = V_{bi} - \left(\frac{\text{ETA} \cdot 8.15^{-22}}{C_{\text{ox}} L_{\text{eff}}^3} \right) v_{DS} + \text{GAMMA} \cdot f_s(\text{PHI} + v_{SB})^{1/2} + f_n(\text{PHI} + v_{SB}) \tag{12}$$

$$v_{bi} = v_{fb} + \text{PHI} \tag{13}$$

or

$$v_{bi} = \text{VTO} - \text{GAMMA} \cdot \sqrt{\text{PHI}} \tag{14}$$

Saturation Voltage

$$v_{sat} = \frac{v_{gs} - V_T}{1 + f_b} \tag{15}$$

$$v_{DS}(\text{sat}) = v_{sat} + v_C - \left(v_{\text{sat}}^2 + v_C^2 \right)^{1/2} \tag{16}$$

$$v_C = \frac{\text{VMAX} \cdot L_{\text{eff}}}{\mu_s} \tag{17}$$

If VMAX is not given, then $v_{DS}(\text{sat}) = v_{sat}$

Effective Mobility

$$\mu_s = \frac{\text{U0}}{1 + \text{THETA}\,(v_{GS} - V_T)} \text{ when VMAX} = 0 \tag{18}$$

$$\mu_{\text{eff}} = \frac{\mu_s}{1 + \frac{v_{DE}}{v_C}} \text{ when VMAX} > 0\text{; otherwise } \mu_{\text{eff}} = \mu_s \tag{19}$$

Channel-Length Modulation

When VMAX = 0

$$\Delta L = xd\left[\text{KAPPA}\ (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{20}$$

when VMAX > 0

$$\Delta L = -\frac{ep \cdot xd^{\,2}}{2} + \left[\left(\frac{ep \cdot xd^{\,2}}{2}\right)^2 + \text{KAPPA} \cdot xd^{\,2} \cdot (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{21}$$

where

$$ep = \frac{v_C\,(v_C + v_{DS}(\text{sat}))}{L_{\text{eff}}\,v_{DS}\,(\text{sat})} \tag{22}$$

$$i_{DS} = \frac{i_{DS}}{1 - \Delta L} \tag{21}$$

Weak Inversion Model (Level 3)

In the SPICE Level 3 model, the transition point from the region of strong inversion to the weak inversion characteristic of the MOS device is designated as v_{on} and is greater than V_T. v_{on} is given by

$$v_{on} = V_T + fast \tag{1}$$

where

$$fast = \frac{kT}{q}\left[1 + \frac{q \cdot NFS}{\text{COX}} + \frac{\text{GAMMA} \cdot f_s\,(\text{PHI} + v_{SB})^{1/2} + f_n\,(\text{PHI} + v_{SB})}{2(\text{PHI} + v_{SB})}\right] \tag{2}$$

NFS is a parameter used in the evaluation of v_{on} and can be extracted from measurements. The drain current in the weak inversion region, v_{GS} less than v_{on}, is given as

$$i_{DS} = i_{DS}\,(v_{on},\, v_{DE},\, v_{SB})\, e^{\left(\frac{v_{GS} - v_{on}}{fast}\right)} \tag{3}$$

Sub

where i_{DS} is given as (from Eq. (1), Sec. 3.4 with v_{GS} replaced with v_{on})

$$i_{DS} = \text{BETA}\left[v_{on} - V_T - \left(\frac{1 + f_b}{2}\right)v_{DE}\right] \cdot v_{DE} \tag{4}$$

Sub-threshold MOS Model:

The models discussed in previous sections predict that no current will flow in a device when the gate–source voltage is at or below the threshold voltage. In reality, this is not the case. As v_{GS} approaches V_T, the $i_D - v_{GS}$ characteristics change from square-law to exponential.

Whereas the region where v_{GS} is above the threshold is called the *strong inversion* region, the region below (actually, the transition between the two regions is not well defined as will be explained later) is called the *subthreshold*, or *weak inversion* region. This is illustrated in Fig. 3.5-1 where the transconductance characteristic of a MOSFET in saturation is shown with the square root of current plotted as a function of the gate–source voltage. When the gate–source voltage reaches the value designated as V_{ON} (this relates to the SPICE model formulation), the current changes from square-law to an exponential-law behavior. It is the objective of this section to present two models suitable for the subthreshold region. The first is the SPICE LEVEL 3 [2] model for computer simulation while the second is useful for hand calculations.

In the SPICE LEVEL 3 model, the transition point from the region of strong inversion to the weak inversion characteristic of the MOS device is designated as V_{ON} and is greater than V_T. V_{ON} is given by

$$V_{ON} = V_T + fast \tag{3.5-1}$$

where

$$fast = \frac{kT}{q}\left[1 + \frac{q \cdot \text{NFS}}{\text{COX}} + \frac{\text{GAMMA} \cdot f_s\,(\text{PHI} + v_{SB})^{1/2} + f_n\,(\text{PHI} + v_{SB})}{2(\text{PHI} + v_{SB})}\right] \tag{3.5-2}$$

NFS is a parameter used in the evaluation of V_{ON} and can be extracted from measurements. The drain current in the weak inversion region, $v_{GS} < V_{ON}$, is given as

$$i_{DS} = i_{DS}\,(V_{ON}, v_{DE}, v_{SB}) \exp\left(\frac{v_{GS} - V_{ON}}{fast}\right) \tag{3.5-3}$$

where i_{DS} is given as [from Eq. (3.4.1), with v_{GS} replaced with V_{ON}]

$$i_{DS} = \text{BETA}\left[V_{ON} - V_T - \left(\frac{1 + f_b}{2}\right)v_{DE}\right] \cdot v_{DE} \tag{3.5-4}$$

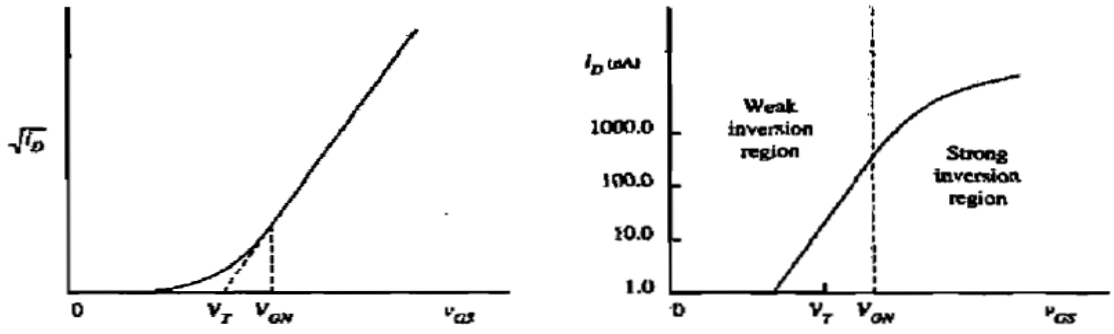


Figure 3.5-1 Weak inversion characteristics of the MOS transistor as modeled by Eq. (3.5-4).

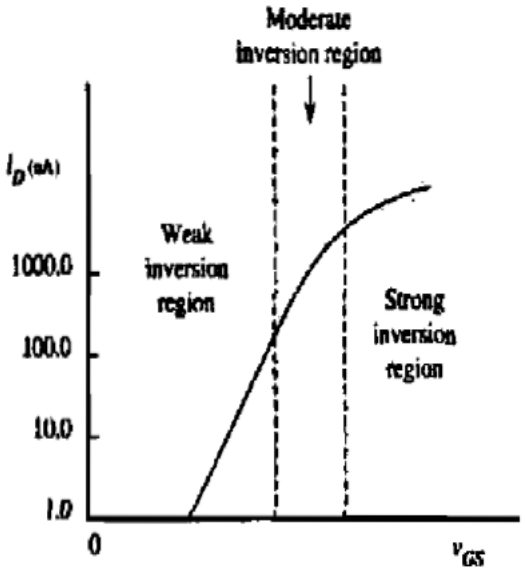


Figure 3.5-2 The three regions of operation of an MOS transistor.

For hand calculations, a simple model describing weak inversion operation is given as

$$i_D \cong \frac{W}{L} I_{D0} \exp\left(\frac{v_{GS}}{n(kT/q)}\right) \tag{3.5-5}$$

where the term n is the subthreshold slope factor, and I_{DO} is a process-dependent parameter that is dependent also on v_{SB} and V_T. These two terms are best extracted from experimental data. Typically n is greater than 1 and less than 3 ($1 < n < 3$). The point at which a transistor enters the weak inversion region can be approximated as

$$v_{gs} < V_T + n\frac{kT}{q} \tag{3.5-6}$$

Unfortunately, the model equations given here do not properly model the transistor as it makes the transition from strong to weak inversion. In reality, there is a transition region of operation between strong and weak inversion called the "moderate inversion" region [15]. This is illustrated in Fig. 3.5-2. A complete treatment of the operation of the transistor through this region is given in the literature [15,16].

It is important to consider the temperature behavior of the MOS device operating in the subthreshold region. As is the case for strong inversion, the temperature coefficient of the threshold voltage is negative in the subthreshold region. The variation of current due to temperature of a device operating in weak inversion is dominated by the negative temperature coefficient of the threshold voltage. Therefore, for a given gate–source voltage, subthreshold current increases as the temperature increases. This is illustrated in Fig. 3.5-3 [17].

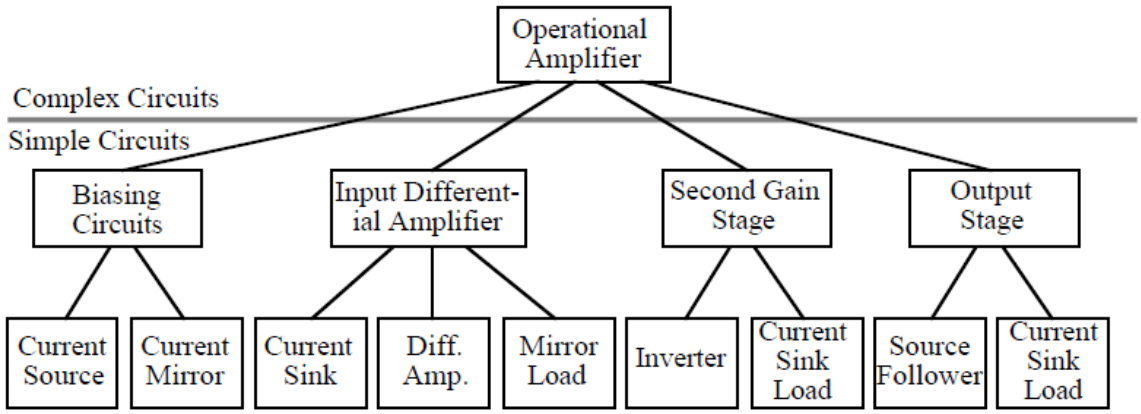
UNIT -II:
Analog CMOS Sub-Circuits

A subcircuit is a circuit which consists of one or more transistors and generally perfoms only one function.

A subcircuit is generally not used by itself but in conjunction with other subcircuits.

Example

Design hierarchy of analog circuits illustrated by an op amp.

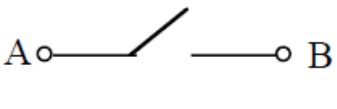


MOS SWITCH:

The switch finds many applications in integrated-circuit design. In analog circuits, the switch is used to implement such useful functions as the switched simulation of a resistor [1]. The switch is also useful for multiplexing, modulation, and a number of other applications. The switch is used as a transmission gate in digital circuits and adds a dimension of flexibility found in standard logic circuits. The objective of this section is to study the characteristics switches that are compatible with CMOS integrated circuits.

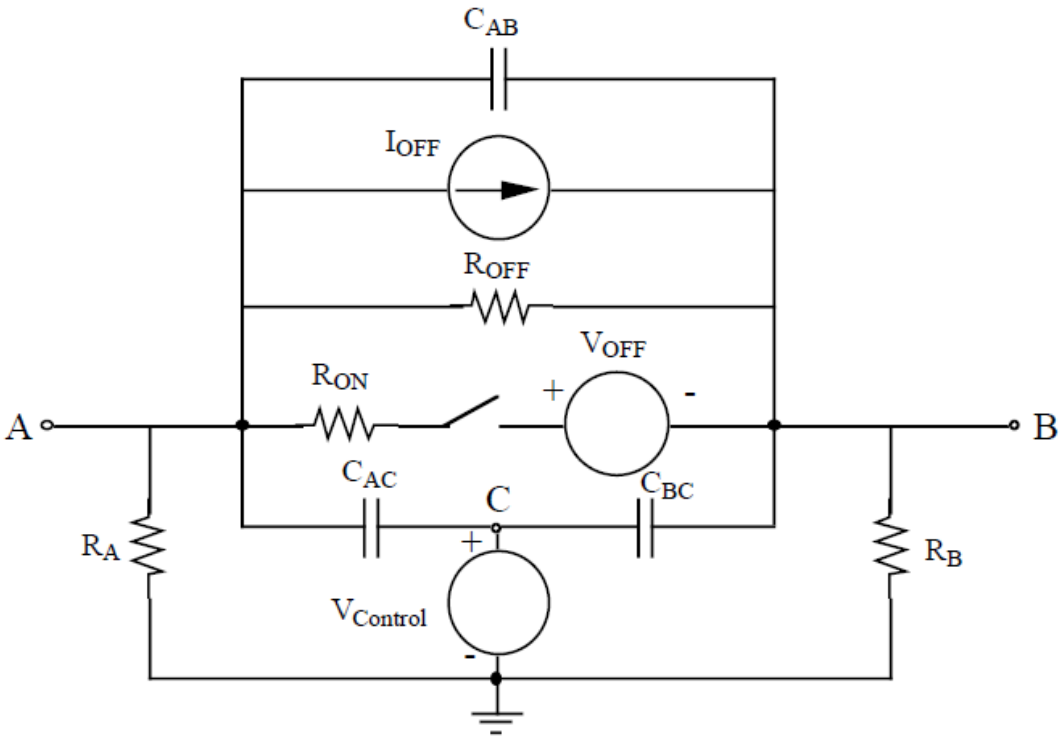
SWITCH PROPERTIES

Ideal Switch



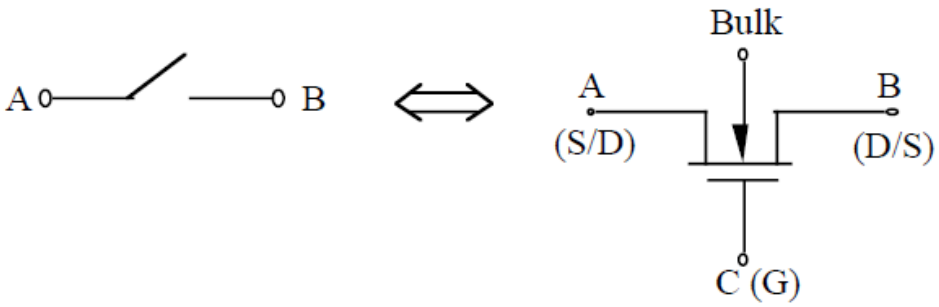
$$\begin{cases} R_{AB}(on) = 0\Omega \\ R_{AB}(off) = \infty \end{cases}$$

Nonideal Switch



MOS TRANSISTOR AS A SWITCH

Symbol



On Characteristics of A MOS Switch

Assume operation in non-saturation region ($v_{DS} < v_{GS} - V_T$).

$$i_D = \frac{K'W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right]v_{DS}$$

$$\frac{\partial i_D}{\partial v_{DS}} = \frac{K'W}{L}\left[v_{GS} - V_T - v_{DS}\right]$$

Thus,

$$R_{ON} = \frac{\partial v_{DS}}{\partial i_D} = \frac{1}{\frac{K'W}{L}(v_{GS} - V_T - v_{DS})}$$

OFF Characteristics of A MOS Switch

If $v_{GS} < V_T$, then $i_D = I_{OFF} = 0$ when $v_{DS} \approx 0V$.

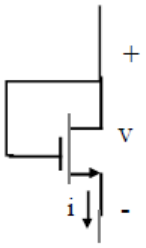
If $v_{DS} > 0$, then

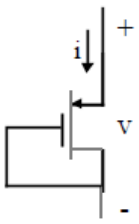
$$R_{OFF} \approx \frac{1}{i_{DS}\lambda} = \frac{1}{I_{OFF}\lambda} \approx \infty$$

MOS DIODE/ACTIVE RESISTOR:

MOS ACTIVE RESISTORS

Realizations





When the drain is connected to the gate, the transistor is always saturated.

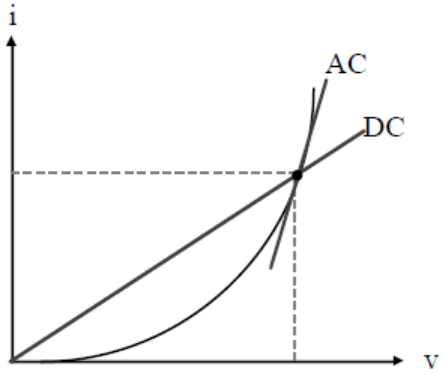
$v_{DS} \geq v_{GS} - V_T$

$v_D - v_S \geq v_G - v_S - V_T$

$\therefore \quad v_{DG} \geq -V_T$ where $V_T > 0$

Large Signal

I-V Characteristics -



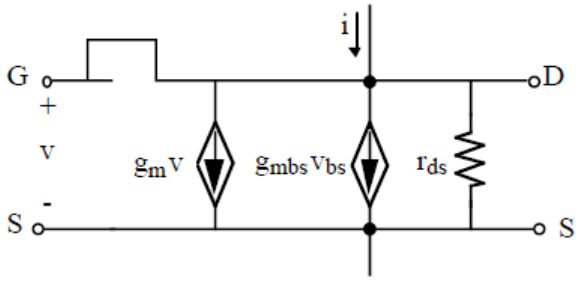
$$i = i_D = \left(\frac{K'W}{2L}\right)[v_{GS} - V_T]^2$$

$$= \frac{\beta}{2}(v_{GS} - V_T)^2, \quad \text{ignore } \lambda$$

or

$$v = v_{DS} = v_{GS} = V_T + \sqrt{\frac{2i_D}{\beta}}$$

Small signal



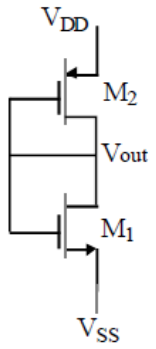
If $V_{BS} = 0$, then $R_{OUT} = \frac{v}{i} = \frac{1}{g_M + g_{DS}} \approx \frac{1}{g_M}$

If $V_{BS} \neq 0$?

Note: Generally, $g_m \approx 10\, g_{mbs} \approx 100\, g_{ds}$

VOLTAGE DIVISION USING ACTIVE RESISTORS

Objective : Derive a voltage Vout from V_{SS} and V_{DD}



Equating i_{D1} to i_{D2} results in :

$$v_{DS1} = \sqrt{\frac{\beta_2}{\beta_1}}\,|v_{DS2} - V_{T2}| + V_{T1}$$

where

$$v_{GS1} = v_{DS1} \quad \text{and} \quad v_{GS2} = v_{DS2}$$

Example :

If $V_{DD} = -V_{SS} = 5$ volts, $V_{out} = 1$ volt, and $I_{D1} = I_{D2} = 50$ µamps, then use the model parameters of Table 3.1-2 to find W/L ratios.

$$i_{D1} = \frac{\beta}{2}(v_{GS} - V_T)^2$$

$\beta_1 = 4.0\ \mu A/V^2$ $\quad \beta_2 = 11.1\ \mu A/V^2$

$K'_n = 17\ \mu A/V^2$ $\quad K'_p = 8\ \mu A/V^2$

$$\text{then} \quad (W/L)_1 = \frac{1}{4.25} \quad \text{and} \quad (W/L)_2 = 1.34$$

SUMMARY OF ACTIVE RESISTOR REALIZATIONS

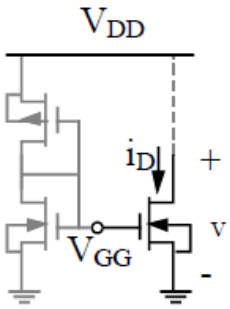
AC Resistance Realization	Linearity	How Controlled	Restrictions
Single MOSFET	Poor	V_{GS} or W/L	$v_{BULK} < \text{Min}\ (v_S, v_D)$
Parallel MOSFET	Good	V_C or W/L	$v \le (V_C - V_T)$
Single-MOSFET, differential resistor	Good	V_C or W/L	$\lvert v_1 \rvert < V_C - V_T$ $v_{BULK} < -v_1$ Differential around v_1
Double-MOSFET, differential resistor	Very Good	$V_{C1} - V_{C2}$ or W/L	$v_1, v_2 < \min(V_{C1}-V_T, V_{C2}-V_T)$ $v_{BULK} < \min(v_1, v_2)$ Transresistance only

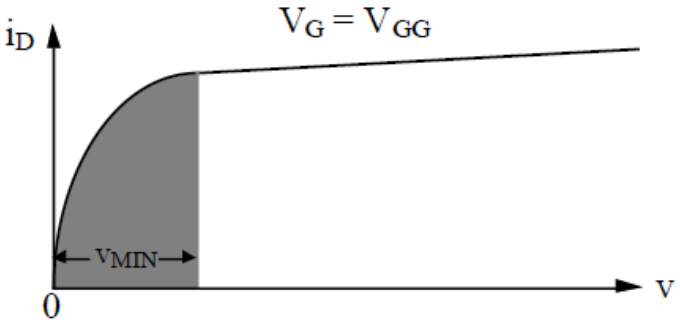
Current Sinks and Sources:

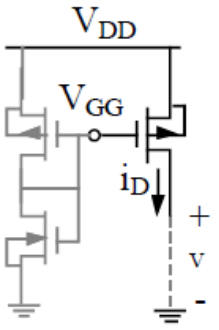
CHARACTERIZATION OF SOURCES & SINKS

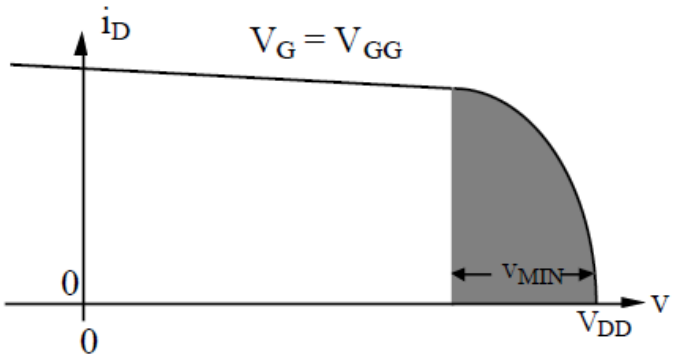
1). Minimum voltage (v_{MIN}) across sink or source for which the current is no longer constant.
2). Output resistance which is a measure of the "flatness" of the current sink or source.

CMOS Current Sinks & Sources





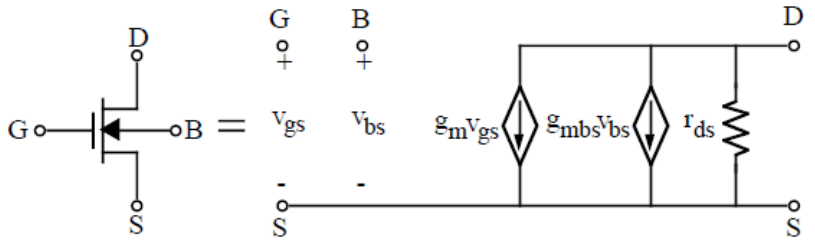




$$r_{OUT} = \frac{1}{\lambda I_D}$$

$v_{MIN} = v_{DS(SAT.)} = v_{ON}$ where $v_{ON} = v_{GS} - V_T$

SMALL SIGNAL MODEL FOR THE MOSFET



$$g_m = \sqrt{\frac{2K'WI_D}{L}}$$

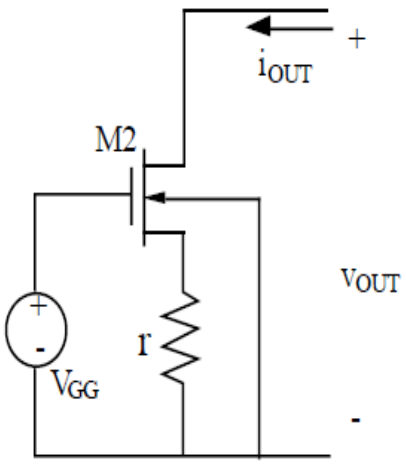
$$g_{mbs} = \frac{g_m \gamma}{2\sqrt{2\phi_F + |V_{BS}|}}$$

$$r_{ds} \approx \frac{1}{g_{ds}} = \frac{1}{\lambda I_D}$$

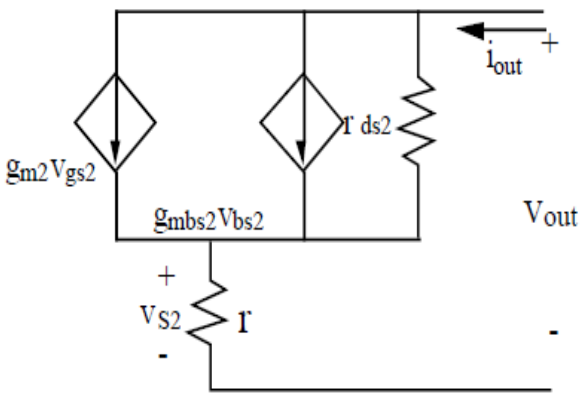
INCREASING THE R_{OUT} OF A CURRENT SOURCE

MOS

Circuit



Small-Signal Model



Loop equation:

$$v_{out} = [i_{out} - (g_{m2}v_{gs2} + g_{mbs2}v_{bs2})]r_{ds2} + i_{out}\, r$$

But, $v_{gs2} = -v_{s2}$ and $v_{bs2} = -\, v_{s2}$.

$$v_{out} = [i_{out} + g_{m2}v_{s2} + g_{mbs2}v_{s2}]r_{ds2} + i_{out}\, r$$

Replace v_{s2} by $i_{out}r$-

$$v_{out} = i_{out}\,[\, r_{ds2} + g_{m2}r_{ds2}r + g_{mbs2}r_{ds2}r + r\,]$$

Therefore,

$$r_{out} = r_{ds2} + r\,[1 + g_{m2}r_{ds2} + g_{mbs2}r_{ds2}]$$

MOS Small Signal Simplifications

Normally,

$$\boxed{g_m \approx 10g_{mbs} \approx 100g_{ds}}$$

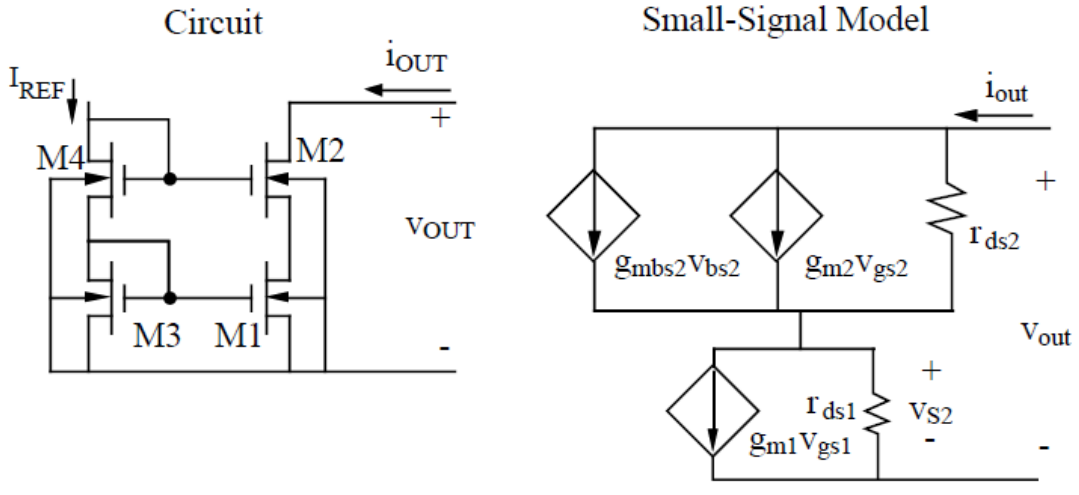
Continuing

$$r_{out} \cong r g_{m2} r_{ds2}$$

r_{out} ≈ r x (voltage gain of M2 from source to drain)

CASCODE CURRENT SINK

MOS



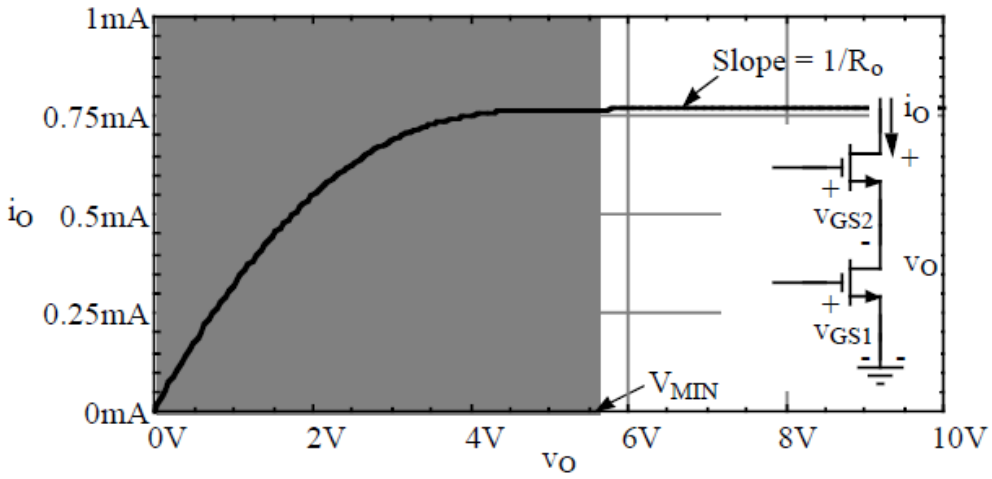
$$v_{out} = [i_{out} - (g_{m2}v_{gs2} + g_{mbs2}v_{bs2})]r_{ds2} + i_{out}r_{ds1}$$

$$v_{out} = i_{out}[r_{ds2} + g_{m2}r_{ds2}r(1 + \eta_2) + r_{ds1}]$$

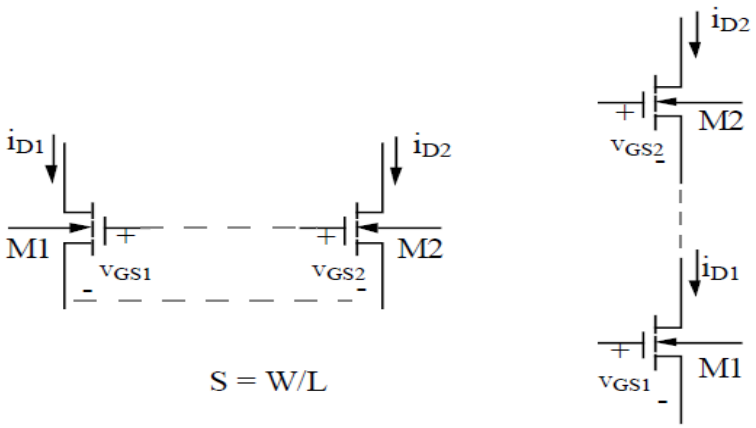
$$r_{out} = r_{ds2} + r[1 + g_{m2}r_{ds2}(1 + \eta_2)] \cong r_{ds1}g_{m2}r_{ds2}(1 + \eta_2)$$

Note : $v_{MIN} = V_T + 2V_{ON} \cong 0.75 + 1.5 = 2.25$ (assuming $V_{ON} \approx V_T$)

NMOS Cascode-



Gate-Source Matching Principle



Assume that M1 and M2 are matched but may not have the same W/L ratios.

1). If $v_{GS1} = v_{GS2}$, then $i_{D1} = (S_1/S_2)i_{D2}$

a). v_{GS1} may be physically connected together , or

b). v_{GS1} may be equal to v_{GS2} by some other means.

2). If $i_{D1} = i_{D2}$, then

a). $v_{GS1} = V_T + \sqrt{S_2/S_1}(v_{GS2} - V_T)$, or

b). If $S_1 = S_2$ and $V_{S1} \approx V_{S2}$ then

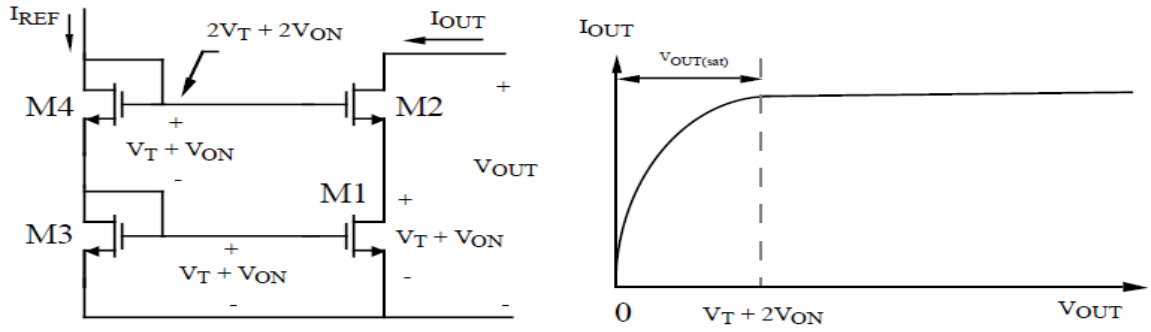
$v_{GS1} = v_{GS2}$

Strictly speaking, absolute matching requires that v_{DS} be equal for two matched devices.

Reduction of V_{MIN} or $V_{OUT}(sat)$

High-Swing Cascode

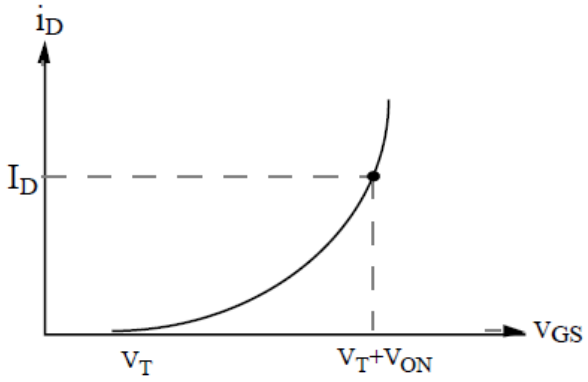
Method 1 for Reducing the Value of $v_{OUT}(sat)$



Standard Cascode Sink :

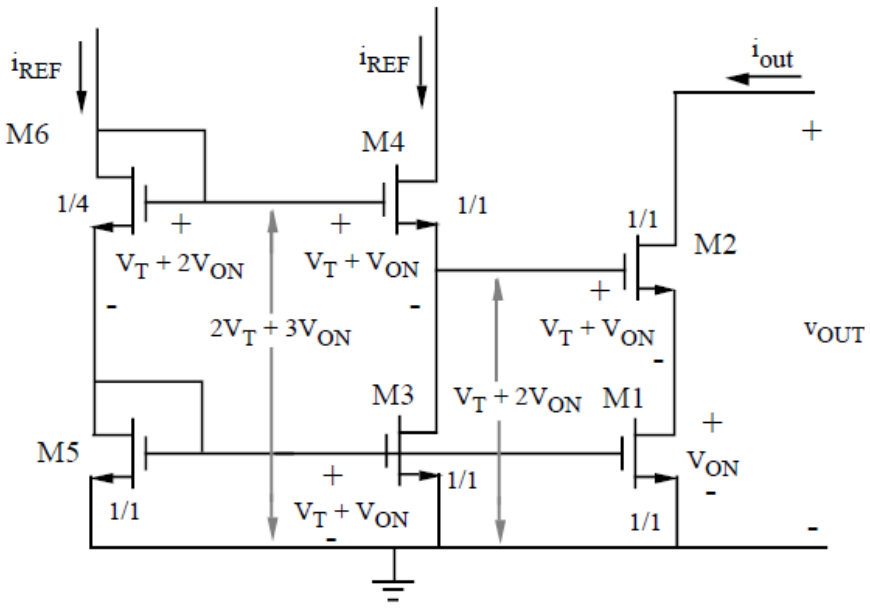
$$v_{GS} = V_{ON} + V_T = \begin{bmatrix}\text{Part of } v_{GS} \\ \text{to achieve} \\ \text{drain current}\end{bmatrix} + \begin{bmatrix}\text{Part of } v_{GS} \text{ to} \\ \text{enhance the channel}\end{bmatrix}$$

$$\therefore \; v_{DS(sat)} = v_{GS} - V_T = (V_{ON} + V_T) - V_T = V_{ON}$$



Above is based on the Gate-Source matching principle.

Circuit Which Reduces the Value of Vout(sat) of the Cascode Current Sink



DESIGNING THE SELF-BIASED HIGH-SWING CASCODE CURRENT SINK FOR A GIVEN V_{MIN}

Use the cascode current-sink configuration of Fig. 4.3-8 to design a current sink of 250 μA and a V_{MIN} of 0.5 V. Assume the device parameters of Table 3.1-2.

Solution

With V_{MIN} of 0.5 V, choose $V_{ON} = 0.25$ V. Using the saturation model, the W/L ratio of M1 and M3 can be found from

$$\frac{W}{L} = \frac{2\, i_{OUT}}{K' V_{ON}^2} = \frac{2 \times 500 \times 10^{-6}}{110 \times 10^{-6} \times 0.0626} = 72.73$$

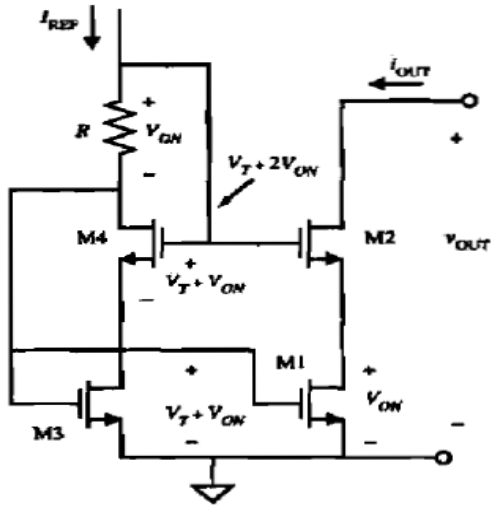


Figure 4.3-8 Self-biased high-swing cascode current source.

The back-gate bias on M2 and M4 is −0.25 V. Therefore, the threshold voltage for M2 and M4 is calculated to be

$$V_{TH} = 0.7 + 0.4\left(\sqrt{0.25 + 0.7} - \sqrt{0.7}\right) = 0.755$$

Taking into account the increased value of the threshold voltage, the gate voltage of M4 and M2 is

$$V_{G4} = 0.755 + 0.25 + 0.25 = 1.255$$

The gate voltage of M1 and M3 is

$$V_{G1} = 0.70 + 0.25 = 0.95$$

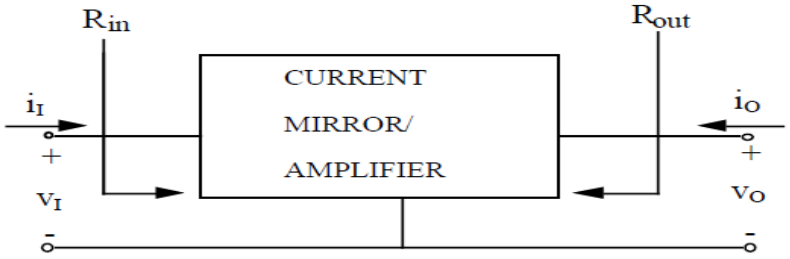
Both terminals of the resistor are now defined so that the required resistance value is easily calculated to be

$$R = \frac{V_{G4} - V_{G1}}{250 \times 10^{-6}} = \frac{1.255 - 0.95}{250 \times 10^{-6}} = 1220\ \Omega$$

Current Mirrors-Current mirror with Beta Helper

Current mirrors are simply an extension of the current sink/source of the previous section. In fact, it is unlikely that one would ever build a current sink/source that was not biased as a current mirror. The current mirror uses the principle that if the gate–source potentials of two identical MOS transistors are equal, the channel currents should be equal. Figure 4.4-1 shows the implementation of a simple n-channel current mirror. The current i_I is assumed to be defined by a current source or some other means and i_O is the output or "mirrored" current. M1 is in saturation because $v_{DS1} = v_{GS1}$. Assuming that $v_{DS2} \geq v_{GS2} - V_{T2}$ is greater than V_{T2} allows us to use the equations in the saturation region of the MOS transistor. In the most general case, the ratio of i_O to i_I is

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right)^2 \left[\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}\left(\frac{K_2'}{K_1'}\right)\right]$$

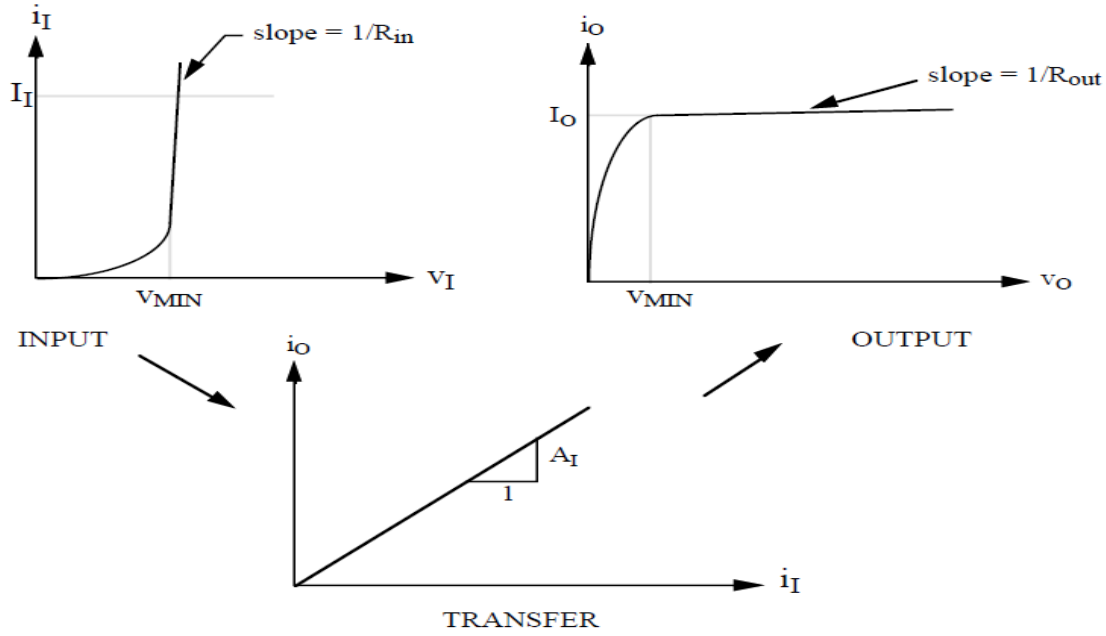


Ideally,

$i_O = A_I\, i_I$

$R_{in} \approx 0 \qquad R_{out} \approx \infty$

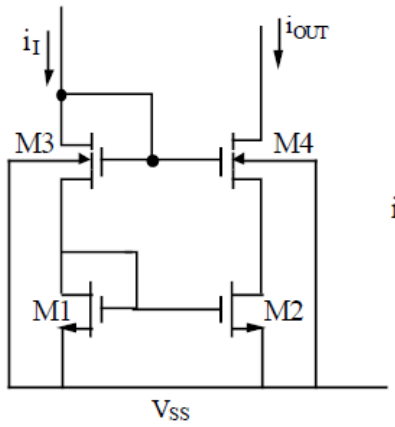
Graphical Characterization



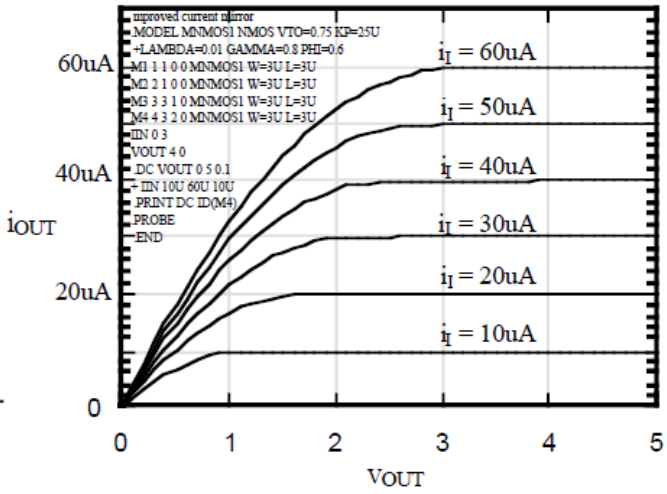
Cascode current Mirror and Wilson Current Mirror

Cadcode Current Mirror

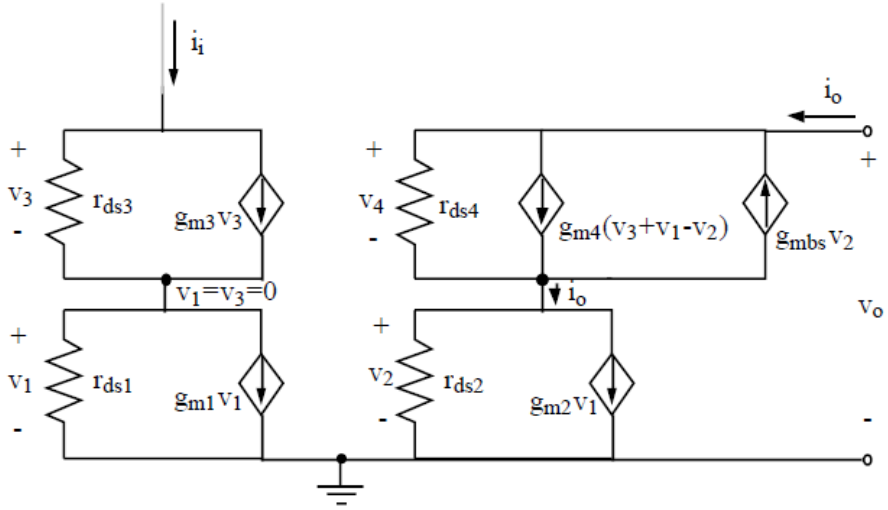
CIRCUIT



SPICE



Example of Small Signal Output Resistance Calculation -



1). $v_o = v_4 + v_2 = r_{ds4}\,[i_o - g_{m4}(v_3 + v_1 - v_2) + g_{mbs4}v_2] + r_{ds2}(i_o - g_{m2}v_1)$

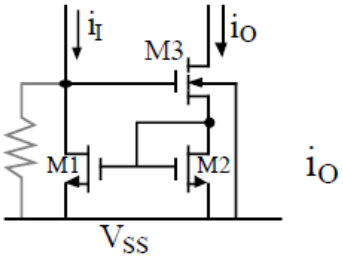
2). $v_2 = i_o r_{ds2}$

3). $v_o = i_o\,[r_{ds4} + (g_{m4}r_{ds2})r_{ds4} + (r_{ds2}g_{mbs4})r_{ds4} + r_{ds2}]$

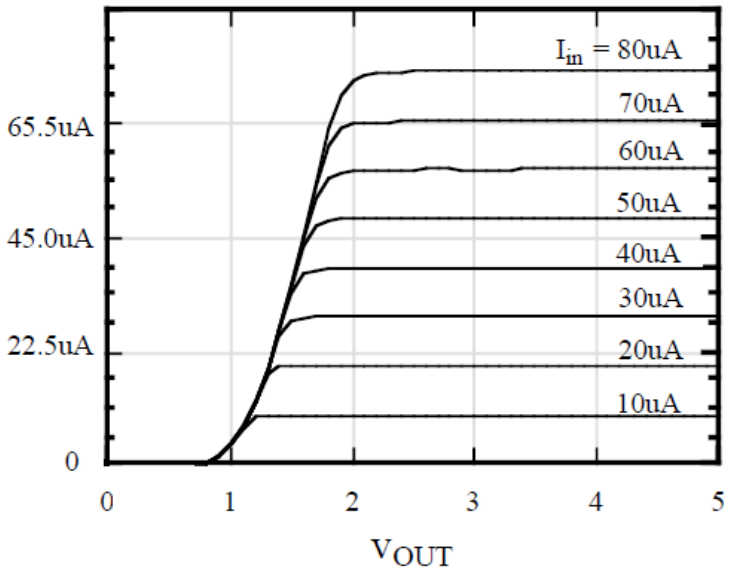
4). $r_{out} = \dfrac{v_o}{i_o} = r_{ds4} + r_{ds2} + r_{ds2}r_{ds4}(g_{m4} + g_{mbs4})$

Wilson Current Mirror

Circuit and Performance-



i_O



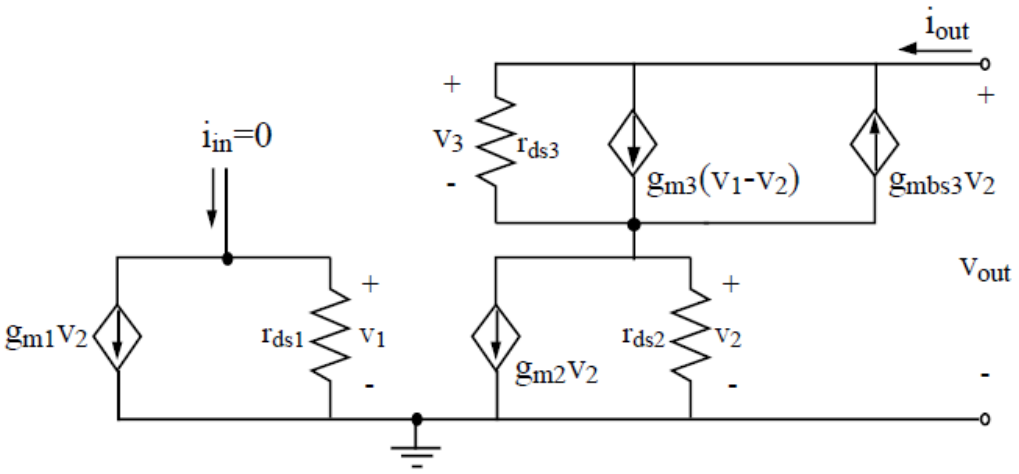

```
Wilson Current Source
M1 1 2 0 0 MNMOS W=15U L=3U
M2 2 2 0 0 MNMOS W=15U L=3U
M3 3 1 2 0 MNMOS W=15U L=3U
R  1 0 100MEG
.MODEL MNMOS NMOS VTO=0.75, KP=25U,
+LAMBDA=0.01, GAMMA=0.8 PHI=0.6
IIN 0 1
VOUT 3 0
.DC VOUT 0 5 0.1 IIN 10U 80U 10U
.PRINT DC  V(2)  V(1) ID(M3)
.PROBE
.END
```

Principle of Operation:

Series negative feedback increase output resistance

1. Assume input current is constant and that there is high resistance to ground from the gate of M3 or drain of M1.
2. A positive increase in output current causes an increase in v_{GS2}.
3. The increase in v_{GS2} causes an increase in v_{GS1}.
4. The increase in v_{GS1} causes an increase in i_{D1}.
5. If the input current is constant, then the current through the resistance to ground from the gate of M3 or the drain of M1 decreases resulting in a decrease in v_{GS3}.
6. A decrease in v_{GS3} causes a decrease in the output current opposing the assumed increase in step 2.

Output Impedance of the Wilson Current Source



$$v_{out} = r_{ds3}[i_{out} - g_{m3}v_1 + g_{m3}v_2 + g_{mbs3}v_2] + v_2$$

$$v_{out} = r_{ds3}i_{out} - g_{m3}r_{ds3}(-g_{m1}r_{ds1}v_2) + g_{m3}r_{ds3}v_2 + g_{mbs3}r_{ds3}v_2 + v_2$$

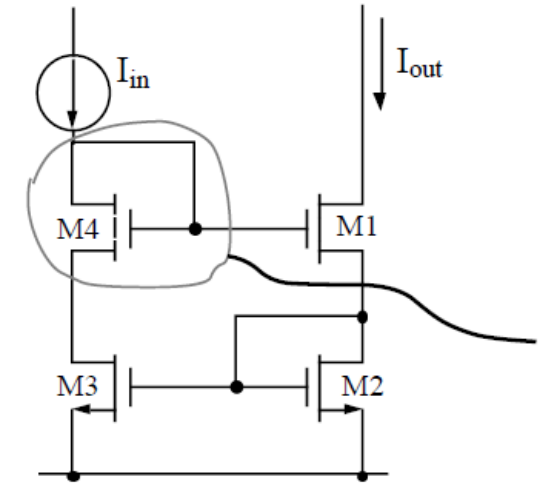
$$v_2 = i_{out}\left[\frac{r_{ds2}}{1 + g_{m2}r_{ds2}}\right]$$

$$v_{out} = i_{out}r_{ds3} + [g_{m3}r_{ds3} + g_{mbs3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3}]v_2 + v_2$$

$$r_{out} = r_{ds3} + r_{ds2}\left[\frac{1 + g_{m3}r_{ds3} + g_{mbs3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1+g_{m2}r_{ds2}}\right]$$

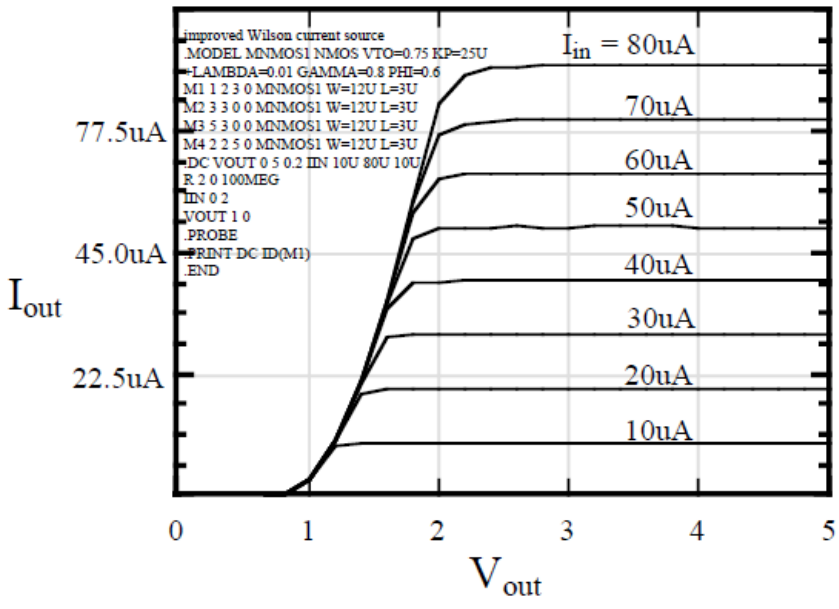
$$\boxed{r_{out} \approx \frac{r_{ds2}g_{m1}r_{ds1}g_{m3}r_{ds3}}{g_{m2}r_{ds2}} \approx r_{ds1} \times (g_{m3}r_{ds3}) \text{ if } g_{m1} = g_{m2}}$$

Improved Wilson Current Mirror



Additional diode-connected transistor equalizes the drain-source voltage drops of transistors M2 and M3

SPICE simulation



SUMMARY OF CURRENT MIRRORS

Current Mirror	Accuracy	Output Resistance	Minimum Voltage
Simple	Poor (Lambda)	r_{ds}	V_{ON}
Cascode	Excellent	$g_m r_{ds}^2$	$V_T + 2V_{ON}$
Wilson	Excellent	$g_m r_{ds}^2$	$2V_{ON}$
Regulated Cascode	Good	$g_m^2 r_{ds}^3$	$V_T + 2V_{ON}$

Current and Voltage References:

An ideal current or voltage reference is independent of power supply and temperature. Many applications in analog circuits require such a building block, which provides a stable current or voltage. The large-signal current and voltage characteristics of an ideal current and voltage reference are shown in Fig. 4.5-1. These characteristics are identical to those of the ideal current and voltage source. The term *reference* is used when the current or voltage values have more precision and stability than ordinarily found in a source. A reference is typically dependent on the load connected to it. It will always be possible to use a buffer amplifier to isolate the reference from the load and maintain the high performance of the reference. In the discussion that follows, it will be assumed that a high-performance voltage reference can be used to implement a high-performance current reference and vice versa.

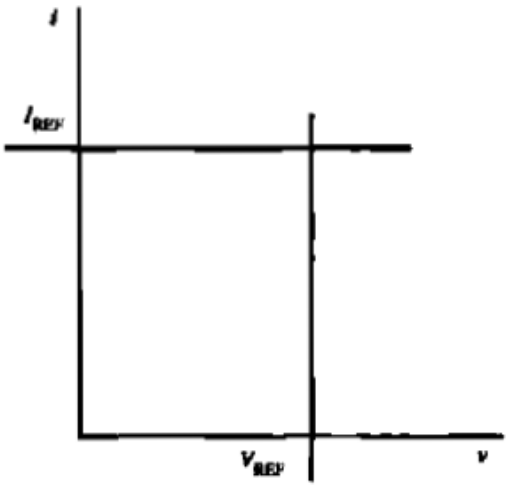


Figure 4.5-1 *I–V* characteristics of ideal current and voltage references.

CALCULATION OF THRESHOLD VOLTAGE REFERENCE CIRCUIT

Calculate the temperature coefficient of the circuit in Fig. 4.5-4(a), where $W/L = 2$, V_{DI} 5 V, and $R = 100\ \text{k}\Omega$, using the parameters of Table 3.1-2. Resistor R is polysilicon and h temperature coefficient of 1500 ppm/°C.

Solution

Using Eq. (4.5-8),

$$V_{REF} = V_T - \frac{1}{\beta_R} + \sqrt{\frac{2(V_{DD} - V_T)}{\beta R} + \frac{1}{\beta^2 R^2}}$$

$$\beta R = 220 \times 10^{-6} \times 10^5 = 22$$

$$V_{REF} = 0.7 - \frac{1}{22} + \sqrt{\frac{2(5 - 0.7)}{22} + \left(\frac{1}{22}\right)^2}$$

$$V_{REF} = 1.281$$

$$\frac{1}{R}\frac{dR}{dT} = 1500\ \text{ppm/°C}$$

$$\frac{dV_{REF}}{dT} = \frac{-\alpha + \sqrt{\frac{V_{DD} - V_{REF}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{1 + \frac{1}{\sqrt{2\beta R\,(V_{DD} - V_{REF})}}}$$

$$\frac{dV_{REF}}{dT} = \frac{-2.3 \times 10^{-3} + \sqrt{\frac{5 - 1.281}{2(22)}}\left(\frac{1.5}{300} - 1500 \times 10^{-6}\right)}{1 + \frac{1}{\sqrt{2(22)\,(5 - 1.281)}}}$$

$$\frac{dV_{REF}}{dT} = -1.189 \times 10^{-3}\ \text{V/°C}$$

The fractional temperature coefficient is given by

$$TC_F = \frac{1}{V_{REF}}\frac{dV_{REF}}{dT}$$

giving, for this example,

$$TC_F = -1.189 \times 10^{-3}\left(\frac{1}{1.281}\right)°C^{-1} = -928\ \text{ppm/°C}$$

Band gap Reference:

In this section we present a technique that results in references that have very little dependence on temperature and power supply. The *bandgap reference* [8–12] can generate references having a temperature coefficient on the order of 10 ppm/°C over the temperature range of 0–70 °C. The principle behind the bandgap reference is illustrated in Fig. 4.6-1. A voltage V_{BE} is generated from a pn-junction diode having a temperature coefficient of approximately −2.2 mV/°C at room temperature. Also generated is a thermal voltage V_t ($= kT/q$), which is proportional to absolute temperature (PTAT) and has a temperature coefficient of +0.085 mV/°C at room temperature. If the V_t voltage is multiplied by a constant K and summed with the V_{BE} voltage, then the output voltage is given as

$$V_{REF} = V_{BE} + KV_t$$

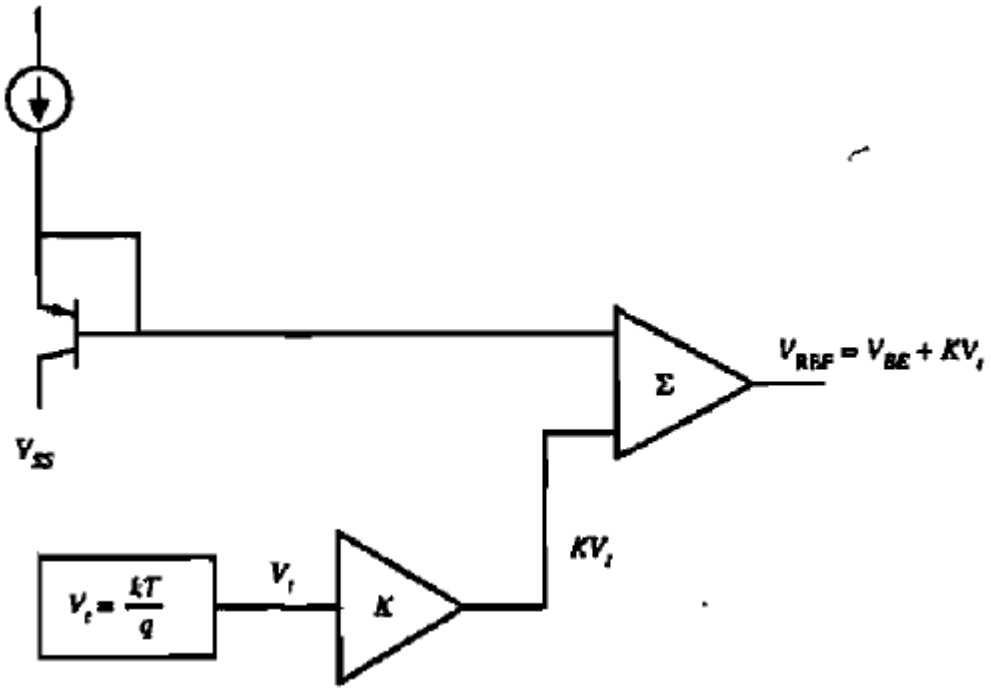


Figure 4.6-1 General principle of the bandgap reference.

To understand thoroughly how the bandgap reference works, we must first develop the temperature dependence of V_{BE}. Consider the relationship for the collector-current density in a bipolar transistor,

$$J_C = \frac{qD_n n_{po}}{W_B} \exp\left(\frac{V_{BE}}{V_t}\right)$$

where

J_C = collector current density (A/m^2)

n_{po} = equilibrium concentration of electrons in the base

D_n = average diffusion constant for electrons

W_B = base width

THE DESIGN OF A BANDGAP-VOLTAGE REFERENCE

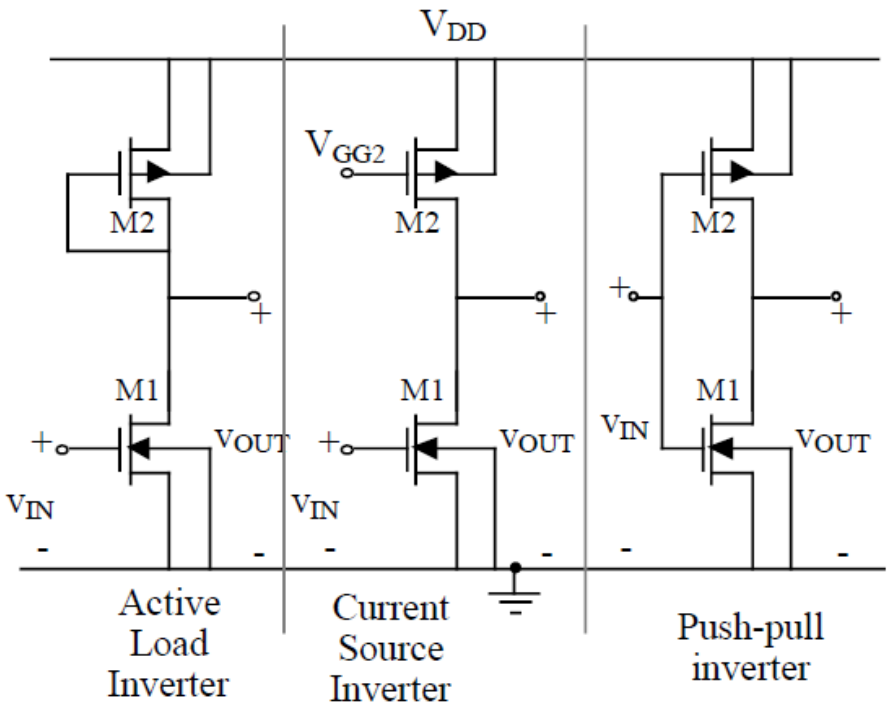
Assume that $A_{E1} = 10\,A_{E2}$, $V_{EB2} = 0.7$ V, $R_2 = R_3$, and $V_t = 0.026$ V at room temperature. Find R_2/R_1 to give a zero temperature coefficient at room temperature.

UNIT -III:
CMOS Amplifiers

Inverters & Differential Amplifiers:

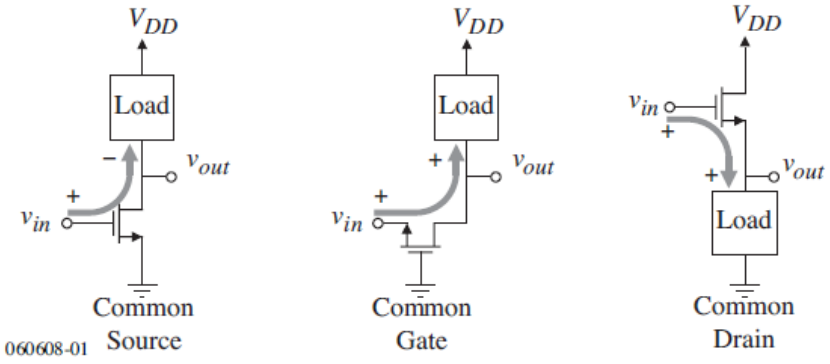
The inverter is the basic gain stage for CMOS circuits. Typically, the inverter uses the common-source configuration with either an active resistor for a load or a current sink/source as a load resistor. There are a number of ways in which the active load can be configured as shown in Fig. 5.1-1. These inverters include the active PMOS load inverter, current-source load inverter, and the push–pull inverter. The small-signal gains increase from left to right in each of these circuits with everything else equal. The active load PMOS inverter, current-source inverter, and push–pull inverter will be considered in this chapter.

Types



Inverting and Noninverting Amplifiers

The types of amplifiers are based on the various configurations of the actual transistors. If we assume that one terminal of the transistor is grounded, then three possibilities result:



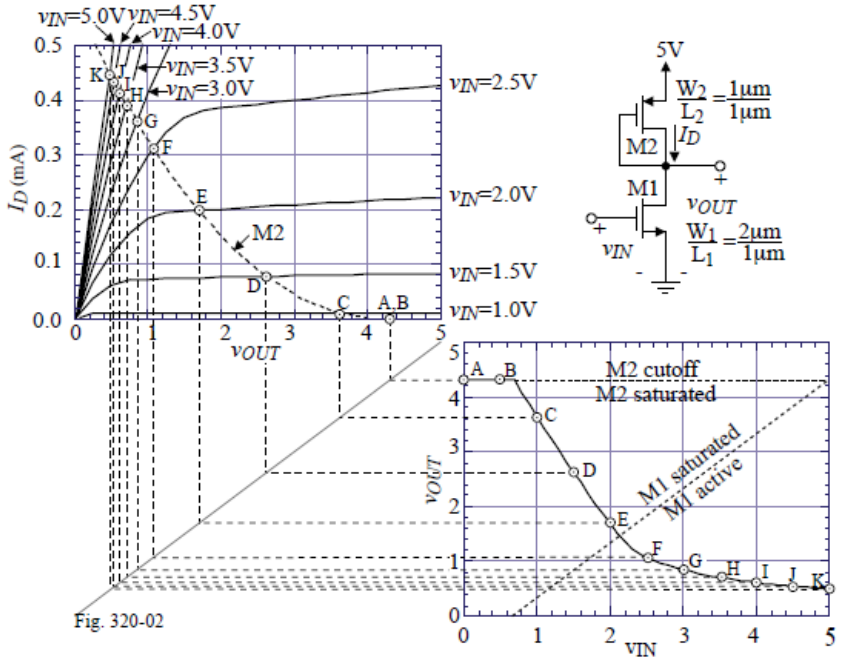
Note that there are two categories of amplifiers:

1.) Noninverting - Those whose input and output are in phase (common gate and common drain)

2.) Inverting - Those whose input and output are out of phase (common source)

ACTIVE LOAD INVERTER

Voltage Transfer Characteristic of the Active Load Inverter



The boundary between active and saturation operation for M1 is

$$v_{DS1} \geq v_{GS1} - V_{TN} \quad \rightarrow \quad v_{OUT} \geq v_{IN} - 0.7\text{V}$$

Large-Signal Voltage Swing Limits of the Active Load Inverter

Maximum output voltage, v_{OUT}(max):

$$v_{OUT}(\max) \cong V_{DD} - |V_{TP}|$$

(ignores subthreshold current influence on the MOSFET)

Minimum output voltage, v_{OUT}(min):

Assume that M1 is nonsaturated and that $V_{T1} = |V_{T2}| = V_T$.

$v_{DS1} \geq v_{GS1} - V_{TN} \quad \rightarrow \quad v_{OUT} \geq v_{IN} - 0.7\text{V}$

The current through M1 is

$$i_D = \beta_1\left((v_{GS1} - V_T)v_{DS1} - \frac{v_{DS1}^2}{2}\right) = \beta_1\left[(V_{DD} - V_T)(v_{OUT}) - \frac{(v_{OUT})^2}{2}\right]$$

and the current through M2 is

$$i_D = \frac{\beta_2}{2}(v_{SG2} - V_T)^2 = \frac{\beta_2}{2}(V_{DD} - v_{OUT} - V_T)^2 = \frac{\beta_2}{2}(v_{OUT} + V_T - V_{DD})^2$$

Equating these currents gives the minimum v_{OUT} as,

$$v_{OUT}(\min) = V_{DD} - V_T - \frac{V_{DD} - V_T}{\sqrt{1 + (\beta_2/\beta_1)}}$$

Small-Signal Midband Performance of the Active Load Inverter

The development of the small-signal model for the active load inverter is shown below:

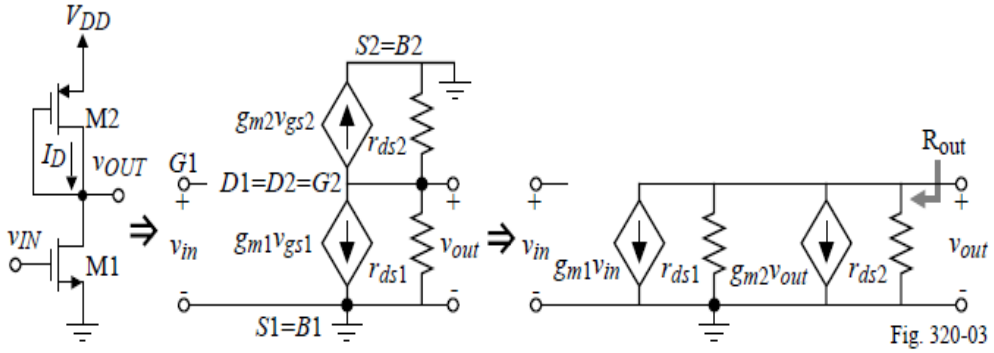


Fig. 320-03

Sum the currents at the output node to get,

$$g_{m1}v_{in} + g_{ds1}v_{out} + g_{m2}v_{out} + g_{ds2}v_{out} = 0$$

Solving for the voltage gain, v_{out}/v_{in}, gives

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \cong -\frac{g_{m1}}{g_{m2}} = -\left(\frac{K'_N W_1 L_2}{K'_P L_1 W_2}\right)^{1/2}$$

The small-signal output resistance can also be found from the above by letting $v_{in} = 0$ to get,

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \cong \frac{1}{g_{m2}}$$

Example 5.1-1 - Performance of an Active Resistor-Load Inverter

Calculate the output-voltage swing limits for V_{DD} = 5 volts, the small-signal gain, the output resistance, and the -3 dB frequency of active load inverter if (W_1/L_1) is 2 μm/1 μm and W_2/L_2 = 1 μm/1 μm, C_{gd1} = 100fF, C_{bd1} = 200fF, C_{bd2} = 100fF, C_{gs2} = 200fF, C_L = 1 pF, and $I_{D1} = I_{D2}$ = 100μA, using the parameters in Table 3.1-2.

Solution

From the above results we find that:

v_{OUT}(max) = 4.3 volts

v_{OUT}(min) = 0.418 volts

Small-signal voltage gain = -1.92V/V

R_{out} = 9.17 kΩ including g_{ds1} and g_{ds2} and 10 kΩ ignoring g_{ds1} and g_{ds2}

z_1 = 2.10x10^9 rads/sec

p_1 = -64.1x10^6 rads/sec.

Thus, the -3 dB frequency is 10.2 MHz.

CURRENT SOURCE INVERTER

Voltage Transfer Characteristic of the Current Source Inverter

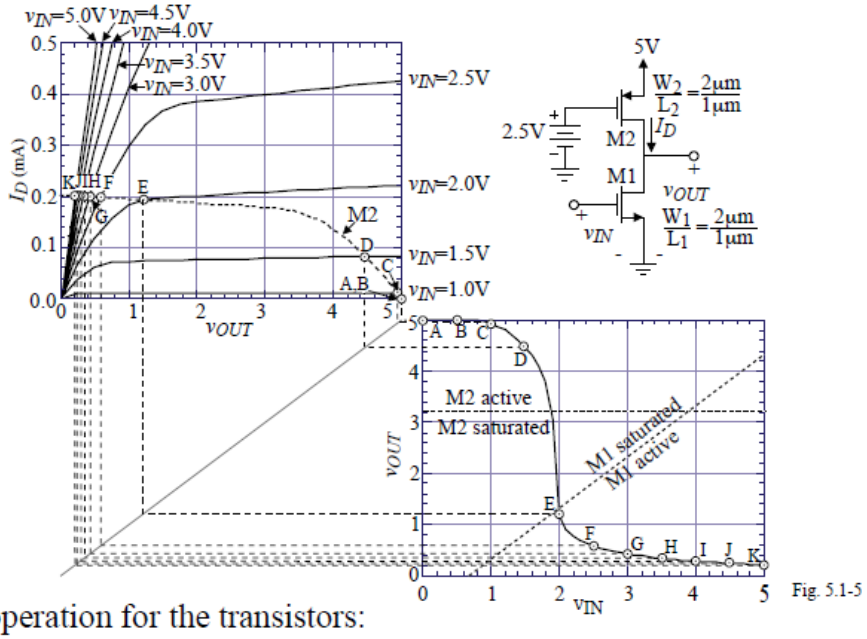


Fig. 5.1-5

Regions of operation for the transistors:

M1: $v_{DS1} \geq v_{GS1} - V_{Tn} \rightarrow v_{OUT} \geq v_{IN} - 0.7V$

M2: $v_{SD2} \geq v_{SG2} - |V_{Tp}| \rightarrow V_{DD} - v_{OUT} \geq V_{DD} - V_{GG2} - |V_{Tp}| \rightarrow v_{OUT} \leq 3.2V$

Frequency Response of the Current Source Load Inverter

Incorporation of the parasitic capacitors into the small-signal model (x is connected to V_{GG2}):

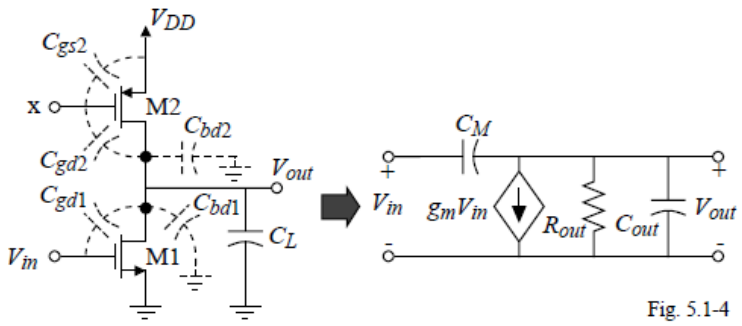


Fig. 5.1-4

If we assume the input voltage has a small source resistance, then we can write the following:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-g_m R_{out}\left(1 - \frac{s}{z_1}\right)}{1 - \frac{s}{p_1}}$$

where $g_m = g_{m1}$, $p_1 = \frac{-1}{R_{out}(C_{out}+C_M)}$, and $z_1 = \frac{g_m}{C_M}$

and $R_{out} = \frac{1}{g_{ds1} + g_{ds2}}$ and $C_{out} = C_{gd2} + C_{bd1} + C_{bd2} + C_L$ $C_M = C_{gd1}$

Therefore, if $|p_1|<|z_1|$, then the –3 dB frequency response can be expressed as

$$\omega_{-3dB} \approx \omega_1 = \frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}$$

Example 5.1-2 - Performance of a Current-Sink Inverter

A current-sink inverter is shown in Fig. 5.1-7. Assume that $W_1 = 2\ \mu$m, $L_1 = 1\ \mu$m, $W_2 = 1\ \mu$m, $L_2 = 1\mu$m, $V_{DD} = 5$ volts, $V_{GG1} = 3$ volts, and the parameters of Table 3.1-2 describe M1 and M2. Use the capacitor values of Example 5.1-1 ($C_{gd1} = C_{gd2}$). Calculate the output-swing limits and the small-signal performance.

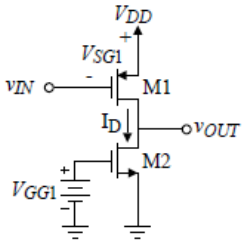


Figure 5.1-7 Current sink CMOS inverter.

Solution

To attain the output signal-swing limitations, we treat Fig. 5.1-7 as a current source CMOS inverter with PMOS parameters for the NMOS and NMOS parameters for the PMOS and use NMOS equations. Using a prime notation to designate the results of the current source CMOS inverter that exchanges the PMOS and NMOS model parameters,

$$v_{OUT}(\text{max})' = 5\text{V and } v_{OUT}(\text{min})' = (5\text{-}0.7)\left[1 - \sqrt{1 - \left(\frac{110\cdot 1}{50\cdot 2}\right)\left(\frac{3\text{-}0.7}{5\text{-}0\text{-}0.7}\right)^2}\right] = 0.74\text{V}$$

In terms of the current sink CMOS inverter, these limits are subtracted from 5V to get

$v_{OUT}(\text{max}) = 4.26\text{V}$ and $v_{OUT}(\text{min}) = 0\text{V}$.

To find the small signal performance, first calculate the dc current. The dc current, I_D, is

$$I_D = \frac{K_N' W_1}{2L_1}(V_{GG1}\text{-}V_{TN})^2 = \frac{110\cdot 1}{2\cdot 1}(3\text{-}0.7)^2 = 291\mu\text{A}$$

$v_{out}/v_{in} = -9.2\text{V/V}$, $R_{out} = 38.1\ \text{k}\Omega$, and $f_{-3dB} = 2.78$ MHz.

Summary of CMOS Inverting Amplifiers

Inverter	AC Voltage Gain	AC Output Resistance	Bandwidth ($C_{GB}=0$)	Equivalent, input-referred,mean-square noise voltage
p-channel active load inverter	$\frac{-g_{m1}}{g_{m2}}$	$\frac{1}{g_{m2}}$	$\frac{g_{m2}}{C_{BD1}+C_{GS1}+C_{GS2}+C_{BD2}}$	$e_{n1}^2 + e_{n2}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2$
Current source load inverter	$\frac{-g_{m1}}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{DG2}+C_{BD2}}$	$e_{n1}^2 + e_{n2}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2$
Push-Pull inverter	$\frac{-(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\left(\frac{g_{m1}e_{n1}}{g_{m1}+g_{m2}}\right)^2+\left(\frac{g_{m1}e_{n1}}{g_{m1}+g_{m2}}\right)^2$

Differential Amplifiers:

CHARACTERIZATION OF A DIFFERENTIAL AMPLIFIER

What is a Differential Amplifier?

A differential amplifier is an amplifier that amplifies the difference between two voltages and rejects the average or common mode value of the two voltages.

Differential and common mode voltages:

v_1 and v_2 are called *single-ended* voltages. They are voltages referenced to ac ground.

The *differential-mode* input voltage, v_{ID}, is the voltage difference between v_1 and v_2.

The *common-mode* input voltage, v_{IC}, is the average value of v_1 and v_2 .

$$\therefore \quad v_{ID} = v_1 - v_2 \quad \text{and} \quad v_{IC} = \frac{v_1+v_2}{2} \quad \Rightarrow \quad v_1 = v_{IC} + 0.5v_{ID} \quad \text{and} \quad v_2 = v_{IC} - 0.5v_{ID}$$

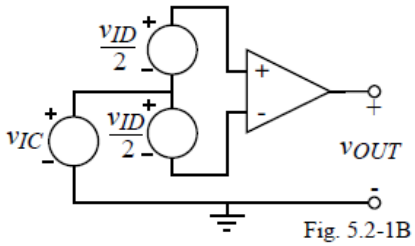


Fig. 5.2-1B

$$v_{OUT} = A_{VD}v_{ID} \pm A_{VC}v_{IC} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)$$

where

A_{VD} = differential-mode voltage gain

A_{VC} = common-mode voltage gain

Differential Amplifier Definitions

• Common mode rejection rato (*CMRR*)

$$CMRR = \left|\frac{A_{VD}}{A_{VC}}\right|$$

CMRR is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

• Input common-mode range (*ICMR*)

The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

• Output offset voltage (V_{OS}(out))

The output offset voltage is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

• Input offset voltage (V_{OS}(in) = V_{OS})

The input offset voltage is equal to the output offset voltage divided by the differential voltage gain.

$$V_{OS} = \frac{V_{OS}(\text{out})}{A_{VD}}$$

Voltage Transfer Characteristic of the Differential Amplifier

In order to obtain the voltage transfer characteristic, a load for the differential amplifier must be defined. We will select a current mirror load as illustrated below.

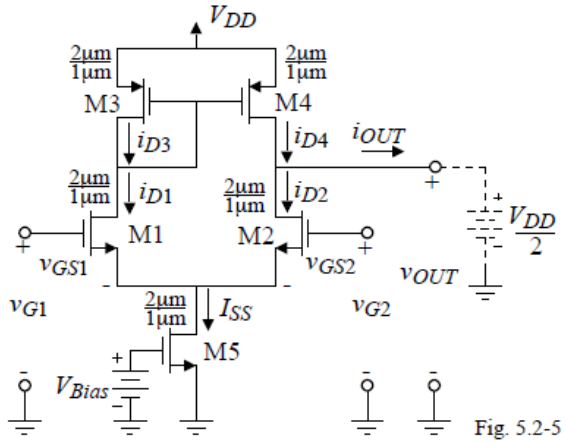


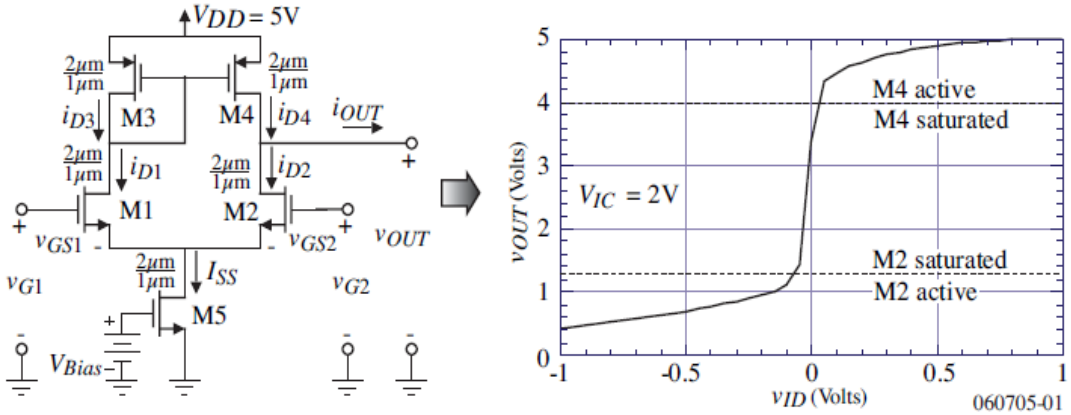
Fig. 5.2-5

Note that output signal to ground is equivalent to the differential output signal due to the current mirror.

The short-circuit, transconductance is given as

$$g_m = \frac{di_{OUT}}{dv_{ID}}(V_{ID}=0) = (\beta I_{SS})^{1/2} = \left(\frac{K'_1 I_{SS} W_1}{L_1}\right)1/2$$

Voltage Transfer Function of the Differential Amplifer with a Current Mirror Load



Regions of operation of the transistors:

M2 is saturated when,

$$v_{DS2} \geq v_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{S1} \geq V_{IC} - 0.5v_{ID} - V_{S1} - V_{TN} \rightarrow v_{OUT} \geq V_{IC} - V_{TN}$$

where we have assumed that the region of transition for M2 is close to $v_{ID} = 0$V.

M4 is saturated when,

$$v_{SD4} \geq v_{SG4} - |V_{TP}| \rightarrow V_{DD} - v_{OUT} \geq V_{SG4} - |V_{TP}| \rightarrow v_{OUT} \leq V_{DD} - V_{SG4} + |V_{TP}|$$

The regions of operations shown on the voltage transfer function assume $I_{SS} = 100\mu$A.

Note: $V_{SG4} = \sqrt{\frac{2 \cdot 50}{50 \cdot 2}} + |V_{TP}| = 1 + |V_{TP}| \Rightarrow \quad v_{OUT} \leq 5 - 1 - 0.7 + 0.7 = 4$V

Frequency Response of the Differential Amplifier

Back to the current mirror load differential amplifier:

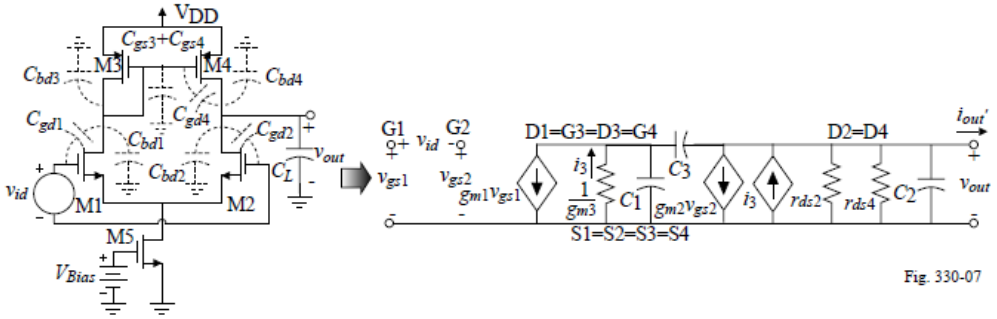


Fig. 330-07

Ignore the zeros that occur due to C_{gd1}, C_{gd2} and C_{gd4}.

$C_1 = C_{gd1}+C_{bd1}+C_{bd3}+C_{gs3}+C_{gs4}$, $C_2 = C_{bd2}+C_{bd4}+C_{gd2}+C_L$ and $C_3 = C_{gd4}$

If $C_3 \approx 0$, then we can write

$$V_{out}(s) \approx \frac{g_{m1}}{g_{ds2}+g_{ds4}}\left[\left(\frac{g_{m3}}{g_{m3}+sC_1}\right)V_{gs1}(s) - V_{gs2}(s)\right]\left(\frac{\omega_2}{s+\omega_2}\right) \quad \text{where } \omega_2 \approx \frac{g_{ds2}+g_{ds4}}{C_2}$$

If we further assume that $g_{m3}/C_1 >> (g_{ds2}+g_{ds4})/C_2 = \omega_2$

then the frequency response of the differential amplifier reduces to

$$\frac{V_{out}(s)}{V_{id}(s)} \cong \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{\omega_2}{s+\omega_2}\right)$$ (A more detailed analysis will be made in Chapter 6)

Noise Analysis of the Differential Amplifier

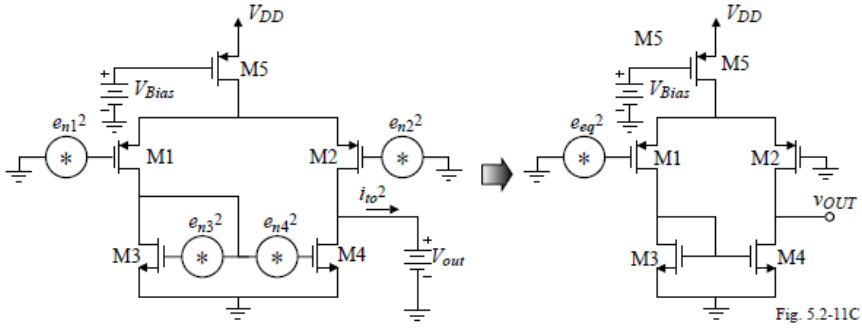


Fig. 5.2-11C

Solve for the total output-noise current to get,

$$i_{to}{}^2 = g_{m1}{}^2e_{n1}{}^2 + g_{m2}{}^2e_{n2}{}^2 + g_{m3}{}^2e_{n3}{}^2 + g_{m4}{}^2e_{n4}{}^2$$

This output-noise current can be expressed in terms of an equivalent input noise voltage, $e_{eq}{}^2$, given as $i_{to}{}^2 = g_{m1}{}^2e_{eq}{}^2$

Equating the above two expressions for the total output-noise current gives,

$$e_{eq}{}^2 = e_{n1}{}^2 + e_{n2}{}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2[e_{n3}{}^2 + e_{n4}{}^2]$$

1/f Noise ($e_{n1}{}^2=e_{n2}{}^2$ and $e_{n3}{}^2=e_{n4}{}^2$):

$$e_{eq(1/f)} = \sqrt{\frac{2B_P}{fW_1L_1}}\sqrt{1+\left(\frac{K'_N B_N}{K'_P B_P}\right)\left(\frac{L_1}{L_3}\right)^2}$$

Thermal Noise ($e_{n1}{}^2=e_{n2}{}^2$ and $e_{n3}{}^2=e_{n4}{}^2$):

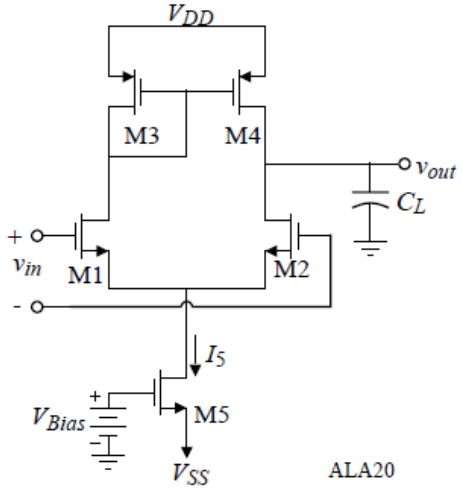
$$e_{eq(th)} = \sqrt{\left(\frac{16kT}{3[2K'_1(W/L)_1I_1]^{1/2}}\right)\left[1+\left(\frac{W_3L_1K'_3}{L_3W_1K'_1}\right)^{1/2}\right]}$$

DESIGNING DIFFERENTIAL AMPLIFIERS

Design of a CMOS Differential Amplifier with a Current Mirror Load

Design Considerations:

Constraints	Specifications
Power supply	Small-signal gain
Technology	Frequency response (C_L)
Temperature	ICMR
	Slew rate (C_L)
	Power dissipation



Relationships

$A_v = g_{m1}R_{out}$

$\omega_{-3dB} = 1/R_{out}C_L$

$V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}$

$V_{IC}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}$

$SR = I_{SS}/C_L$

$P_{diss} = (V_{DD}+|V_{SS}|)$xAll dc currents flowing from V_{DD} or to V_{SS}

Example 5.2-2 - Design of a MOS Differential Amp. with a Current Mirror Load

Design the currents and W/L values of the current mirror load MOS differential amplifier to satisfy the following specifications: $V_{DD} = -V_{SS} = 2.5$V, $SR \geq 10$V/μs (C_L=5pF), $f_{-3dB} \geq 100$kHz (C_L=5pF), a small signal gain of 100V/V, -1.5V$\leq ICMR \leq$2V and $P_{diss} \leq 1$mW. Use the parameters of K_N'=110μA/V^2, K_P'=50μA/V^2, V_{TN}=0.7V, V_{TP}=-0.7V, λ_N=0.04V^{-1} and λ_P=0.05V^{-1}.

Solution

1.) To meet the slew rate, $I_{SS} \geq 50\mu$A. For maximum P_{diss}, $I_{SS} \leq 200\mu$A.

2.) f_{-3dB} of 100kHz implies that $R_{out} \leq 318$kΩ. Therefore $R_{out} = \dfrac{2}{(\lambda_N+\lambda_P)I_{SS}} \leq 318$kΩ

$\therefore\ I_{SS} \geq 70\mu$A Thus, pick $I_{SS} = 100\mu$A

3.) $V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1} \rightarrow 2\text{V} = 2.5 - V_{SG3} + 0.7$

$$V_{SG3} = 1.2\text{V} = \sqrt{\frac{2\cdot 50\mu\text{A}}{50\mu\text{A/V}^2(W_3/L_3)}} + 0.7$$

$$\therefore\ \frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{2}{(0.5)^2} = 8$$

4.) $$100 = g_{m1}R_{out} = \frac{g_{m1}}{g_{ds2}+g_{ds4}} = \frac{\sqrt{2\cdot 110\mu\text{A/V}^2(W_1/L_1)}}{(0.04+0.05)\sqrt{50\mu\text{A}}} = 23.31\sqrt{\frac{W_1}{L_1}} \rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = 18.4$$

5.) $V_{IC}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} \rightarrow -1.5 = -2.5 + V_{DS5}(\text{sat}) + \sqrt{\frac{2 \cdot 50\mu\text{A}}{110\mu\text{A/V}^2(18.4)}} + 0.7$

$V_{DS5}(\text{sat}) = 0.3 - 0.222 = 0.0777 \Rightarrow \frac{W_5}{L_5} = \frac{2I_{SS}}{K_N' V_{DS5}(\text{sat})^2} = 150.6$

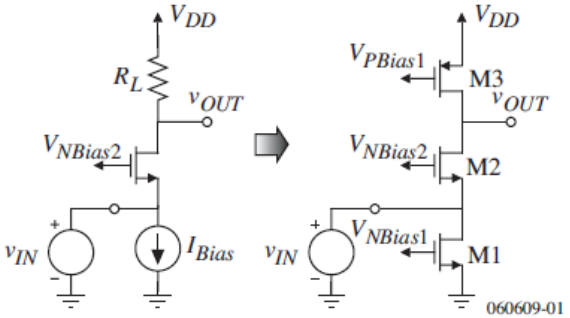
We probably should increase W_1/L_1 to reduce V_{GS1}. If we choose $W_1/L_1 = 40$, then $V_{DS5}(\text{sat}) = 0.149\text{V}$ and $W_5/L_5 = 41$. (Larger than specified gain should be okay.)

Cascode Amplifiers :

VOLTAGE-DRIVEN COMMON GATE AMPLIFIER

Common Gate Amplifier

Circuit:

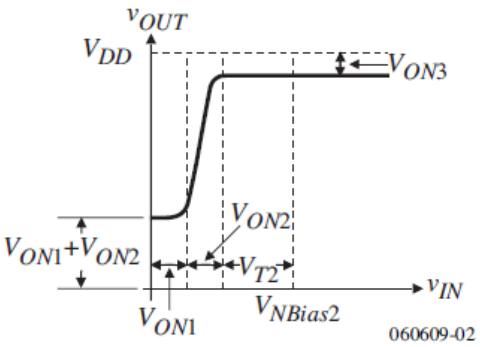


Large Signal Characteristics:

$V_{OUT}(\max) \approx V_{DD} - V_{DS3}(\text{sat})$

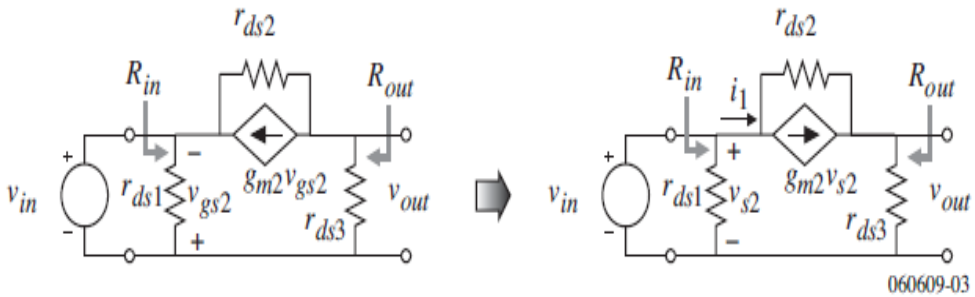
$V_{OUT}(\min) \approx V_{DS1}(\text{sat}) + V_{DS2}(\text{sat})$

Note $V_{DS1}(\text{sat}) = V_{ON1}$



Small Signal Performance of the Common Gate Amplifier

Small signal model:



$$v_{out} = g_{m2}v_{s2}\left(\frac{r_{ds2}}{r_{ds2}+r_{ds3}}\right)r_{ds3} = \left(\frac{g_{m2}r_{ds2}r_{ds3}}{r_{ds2}+r_{ds3}}\right)v_{in} \quad \rightarrow \boxed{A_v = \frac{v_{out}}{v_{in}} = +\frac{g_{m2}r_{ds2}r_{ds3}}{r_{ds2}+r_{ds3}}}$$

$R_{in} = R_{in}' \| r_{ds1}$, R_{in}' is found as follows

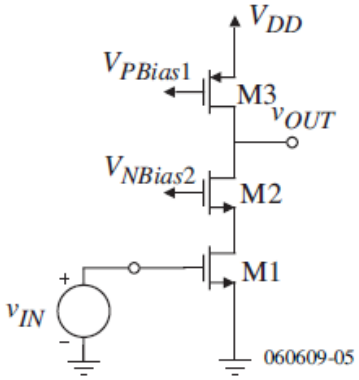
$$v_{s2} = (i_1 - g_{m2}v_{s2})r_{ds2} + i_1 r_{ds3} = i_1(r_{ds2} + r_{ds3}) - g_{m2}\, r_{ds2}v_{s2}$$

$$R_{in}' = \frac{v_{s2}}{i_1} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2}r_{ds2}} \quad \rightarrow \quad \boxed{R_{in} = r_{ds1} \| \frac{r_{ds2} + r_{ds3}}{1 + g_{m2}r_{ds2}}}$$

$$\boxed{R_{out} \approx r_{ds2} \| r_{ds3}}$$

VOLTAGE-DRIVEN CASCODE AMPLIFIER

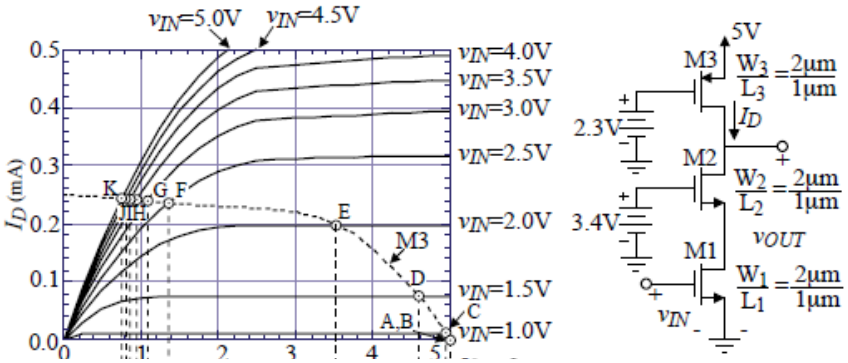
Cascode Amplifier



Advantages of the cascode amplifier:

- Increases the output resistance and gain (if M3 is cascaded also)
- Eliminates the Miller effect when the input source resistance is large

Large-Signal Characteristics of the Cascode Amplifier



Frequency Response of the Cascode Amplifier

Small-signal model ($R_S = 0$):

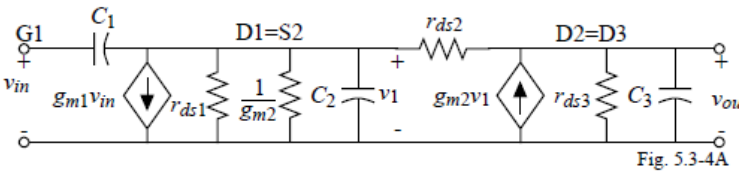


Fig. 5.3-4A

where

$C_1 = C_{gd1}$,

$C_2 = C_{bd1}+C_{bs2}+C_{gs2}$, and

$C_3 = C_{bd2}+C_{bd3}+C_{gd2}+C_{gd3}+C_L$

The nodal equations now become:

$$(g_{m2} + g_{ds1} + g_{ds2} + sC_1 + sC_2)v_1 - g_{ds2}v_{out} = -(g_{m1} - sC_1)v_{in}$$

and $$-(g_{ds2} + g_{m2})v_1 + (g_{ds2} + g_{ds3} + sC_3)v_{out} = 0$$

Solving for $V_{out}(s)/V_{in}(s)$ gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{1}{1 + as + bs^2}\right)\left(\frac{-(g_{m1} - sC_1)(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}\right)$$

where

$$a = \frac{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}$$

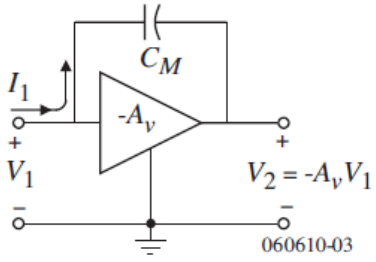
and

$$b = \frac{C_3(C_1 + C_2)}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}$$

NON-VOLTAGE DRIVEN CASCODE AMPLIFIER – THE MILLER EFFECT

Miller Effect

Consider the following inverting amplifier:



Solve for the input impedance:

$$Z_{in}(s) = \frac{V_1}{I_1}$$

$$I_1 = sC_M(V_1 - V_2) = sC_M(V_1 + A_vV_1) = sC_M(1 + A_v)V_1$$

Therefore,

$$Z_{in}(s) = \frac{V_1}{I_1} = \frac{V_1}{sC_M(1 + A_v)V_1} = \frac{1}{sC_M(1 + A_v)} = \frac{1}{sC_{eq}}$$

The Miller effect can take C_{gd} = 5fF and make it look like a 0.5pF capacitor in parallel with the input of the inverting amplifier ($A_v \approx$ -100).

If the source resistance is large, this creates a dominant pole at the input.

Designing Cascode Amplifiers

Pertinent design equations for the simple cascode amplifier.

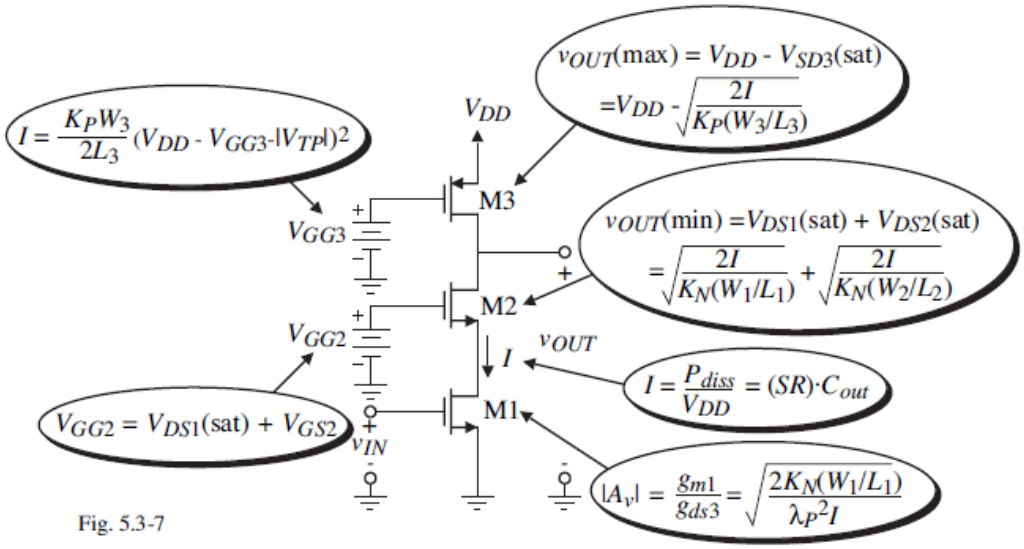


Fig. 5.3-7

Example 5.3-3 - Design of a Cascode Amplifier

The specs for a cascode amplifier are $A_v = -50$V/V, $v_{OUT}(\max) = 4$V, $v_{OUT}(\min) = 1.5$V, V_{DD}=5V, and P_{diss}=1mW. The slew rate with a 10pF load should be 10V/μs or greater.

Solution

The slew rate requires a current greater than 100μA while the power dissipation requires a current less than 200μA. Compromise with 150μA. Beginning with M3,

$$\frac{W_3}{L_3} = \frac{2I}{K_P[V_{DD} - v_{OUT}(\max)]^2} = \frac{2\cdot 150}{50(1)^2} = 6$$

From this find V_{GG3}: $V_{GG3} = V_{DD} - |V_{TP}| - \sqrt{\frac{2I}{K_P(W_3/L_3)}} = 5 - 1 - \sqrt{\frac{2\cdot 150}{50\cdot 6}} = 3\text{V}$

Next, $$\frac{W_1}{L_1} = \frac{(A_v\lambda)^2 I}{2K_N} = \frac{(50\cdot 0.05)^2(150)}{2\cdot 110} = 2.73$$

To design W_2/L_2, we will first calculate V_{DS1}(sat) and use the v_{OUT}(min) specification to define V_{DS2}(sat). $V_{DS1}(\text{sat}) = \sqrt{\frac{2I}{K_N(W_1/L_1)}} = \sqrt{\frac{2\cdot 150}{110\cdot 4.26}} = 0.8\text{V}$

Subtracting this value from 1.5V gives $V_{DS2}(\text{sat}) = 0.7$V.

$$\therefore \quad \frac{W_2}{L_2} = \frac{2I}{K_N V_{DS2}(\text{sat})^2} = \frac{2\cdot 150}{110\cdot 0.7^2} = 5.57$$

Finally, $V_{GG2} = V_{DS1}(\text{sat}) + \sqrt{\frac{2I}{K_N(W_2/L_2)}} + V_{TN} = 0.8\text{V} + 0.7\text{V} + 0.7\text{V} = 2.2\text{V}$

Current Amplifiers:

- An amplifier that has a defined output-input current relationship
- Low input resistance
- High output resistance

Application of current amplifiers:

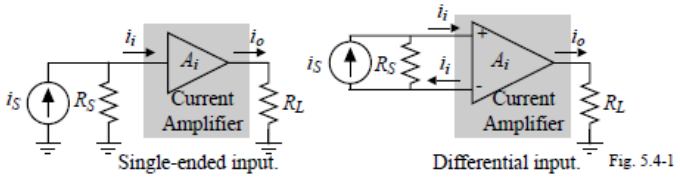


Fig. 5.4-1

$R_S >> R_{in}$ and $R_{out} >> R_L$

Advantages of current amplifiers:

- Currents are not restricted by the power supply voltages so that wider dynamic ranges are possible with lower power supply voltages.
- -3dB bandwidth of a current amplifier using negative feedback is independent of the closed loop gain.

Frequency Response of a Current Amplifier with Current Feedback

Consider the following current amplifier with resistive negative feedback applied.

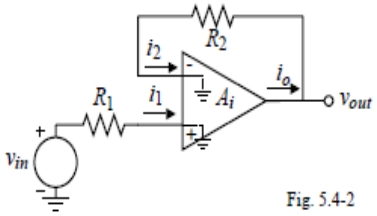


Fig. 5.4-2

Assuming that the small-signal resistance looking into the current amplifier is much less than R_1 or R_2,

$$i_o = A_i(i_1 - i_2) = A_i\left(\frac{v_{in}}{R_1} - i_o\right)$$

Solving for i_o gives

$$i_o = \left(\frac{A_i}{1+A_i}\right)\frac{v_{in}}{R_1} \quad \rightarrow \quad v_{out} = R_2 i_o = \frac{R_2}{R_1}\left(\frac{A_i}{1+A_i}\right)v_{in}$$

If $A_i(s) = \dfrac{A_o}{\dfrac{s}{\omega_A} + 1}$, then

$$\frac{v_{out}}{v_{in}} = \frac{R_2}{R_1}\left(\frac{1}{1+\dfrac{1}{A_i(s)}}\right) = \frac{R_2}{R_1}\left(\frac{A_o}{\dfrac{s}{\omega_A}+(1+A_o)}\right) = \frac{R_2}{R_1}\left(\frac{A_o}{1+A_o}\right)\left(\frac{1}{\dfrac{s}{\omega_A(1+A_o)}+1}\right)$$

$\therefore \quad \omega_{-3dB} = \omega_A(1+A_o)$

Bandwidth Advantage of a Current Feedback Amplifier

The unity-gainbandwidth is,

$$GB = |A_v(0)|\ \omega_{-3dB} = \frac{R_2 A_o}{R_1(1+A_o)} \cdot \omega_A(1+A_o) = \frac{R_2}{R_1} A_o \cdot \omega_A = \frac{R_2}{R_1} GB_i$$

where GB_i is the unity-gainbandwidth of the current amplifier.

Note that if GB_i is constant, then increasing R_2/R_1 (the voltage gain) increases GB.

Illustration:

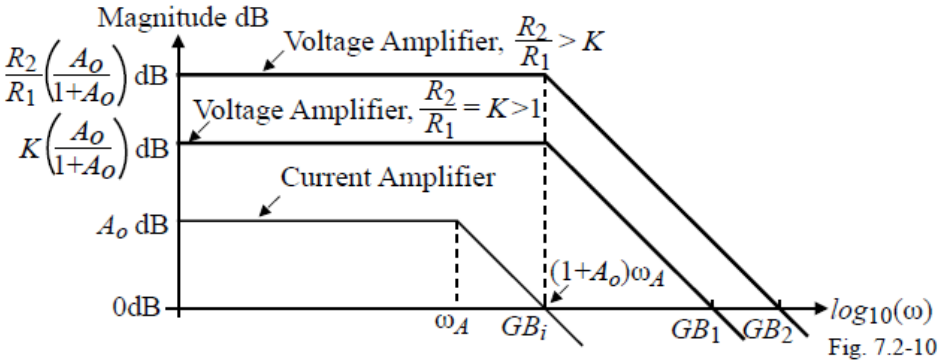


Fig. 7.2-10

Note that $GB_2 > GB_1 > GB_i$

The above illustration assumes that the GB of the voltage amplifier realizing the voltage buffer is greater than the GB achieved from the above method.

Current Amplifier using the Simple Current Mirror

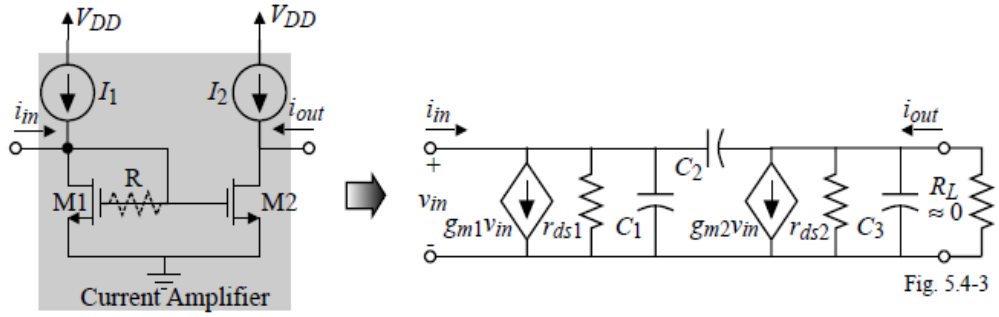


Fig. 5.4-3

$$R_{in} = \frac{1}{g_{m1}} \quad R_{out} = \frac{1}{\lambda_1 I_o} \qquad \text{and} \qquad A_i = \frac{W_2/L_2}{W_1/L_1}\ .$$

Frequency response:

$$p_1 = \frac{-(g_{m1}+g_{ds1})}{C_1+C_2} = \frac{-(g_{m1}+g_{ds1})}{C_{bd1}+C_{gs1}+C_{gs2}+C_{gd2}} \approx \frac{-g_{m1}}{C_{bd1}+C_{gs1}+C_{gs2}+C_{gd2}}$$

Note that the bandwidth can be almost doubled by including the resistor, R.
(R removes C_{gs1} from p_1)

Example 5.4-1- Performance of a Simple Current Mirror as a Current Amplifier

Find the small-signal current gain, A_i, the input resistance, R_{in}, the output resistance, R_{out}, and the -3dB frequency in Hertz for the current amplifier of Fig. 5.4-3(a) if $10I_1 = I_2 = 100\mu$A and $W_2/L_2 = 10W_1/L_1 = 10\mu$m/1$\mu$m. Assume that $C_{bd1} = 10$fF, $C_{gs1} = C_{gs2} = 100$fF, and $C_{gs2} = 50$fF.

Solution

Ignoring channel modulation and mismatch effects, the small-signal current gain,

$$A_i = \frac{W_2/L_2}{W_1/L_1} \approx 10\text{A/A}.$$

The small-signal input resistance, R_{in}, is approximately $1/g_{m1}$ and is

$$R_{in} \approx \frac{1}{\sqrt{2K_N(1/1)10\mu\text{A}}} = \frac{1}{46.9\mu\text{S}} = 21.3\text{k}\Omega$$

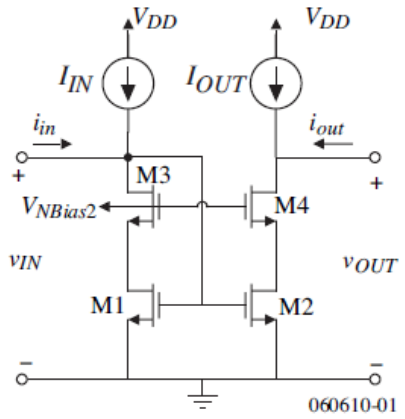
The small-signal output resistance is equal to

$$R_{out} = \frac{1}{\lambda_N I_2} = 250\text{k}\Omega.$$

The -3dB frequency is

$$\omega_{\text{-3dB}} = \frac{46.9\mu\text{S}}{260\text{fF}} = 180.4\text{x}10^6 \text{ radians/sec.} \quad \rightarrow \quad f_{\text{-3dB}} = 28.7 \text{ MHz}$$

Wide-Swing, Cascode Current Mirror Implementation of a Current Amplifier



$$R_{in} \approx \frac{1}{g_{m1}}, \quad R_{out} \approx r_{ds2}g_{m4}r_{ds4}, \quad \text{and} \quad A_i = \frac{W_2/L_2}{W_1/L_1}$$

Differential-Input, Current Amplifiers

Definitions for the differential-mode, i_{ID}, and common-mode, i_{IC}, input currents of the differential-input current amplifier.

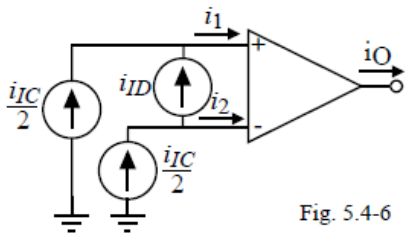
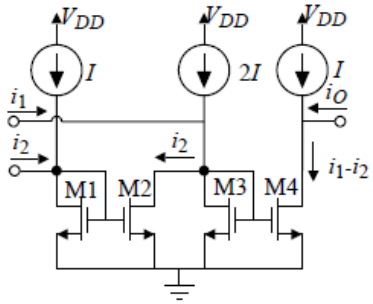


Fig. 5.4-6

$$i_o = A_{ID} i_{ID} \pm A_{IC} i_{IC} = A_{ID}(i_1 - i_2) \pm A_{IC}\left(\frac{i_1+i_2}{2}\right)$$

Implementations:



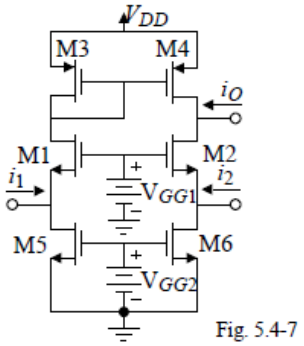


Fig. 5.4-7

Summary

- Current amplifiers have a low input resistance, high output resistance, and a defined output-input current relationship
- Input resistances less than $1/g_m$ require feedback

  However, all feedback loops have internal poles that cause the benefits of negative feedback to vanish at high frequencies.

  In addition, these feedback loops can have a slow time constant from a pole-zero pair.
- Voltage amplifiers using a current amplifier have high values of gain-bandwidth
- Current amplifiers are useful at low power supplies and for switched current applications

Output Amplifiers:

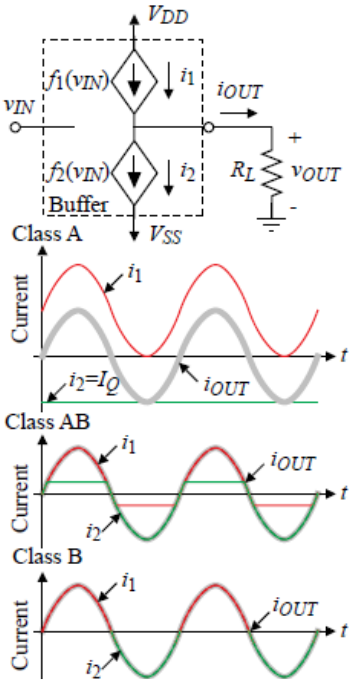
General Considerations of Output Amplifiers

Requirements:

1.) Provide sufficient output power in the form of voltage or current.
2.) Avoid signal distortion.
3.) Be efficient
4.) Provide protection from abnormal conditions (short circuit, over temperature, etc.)

Types of Output Amplifiers:

1.) Class A amplifiers
2.) Source followers
3.) Push-pull amplifiers
4.) Substrate BJT amplifiers
5.) Amplifiers using negative shunt feedback



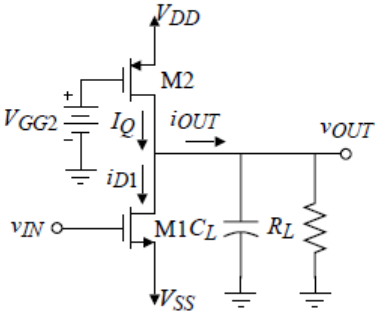
CLASS A AMPLIFIERS

Current source load inverter

A Class A circuit has current flow in the MOSFETs during the entire period of a sinusoidal signal.

Characteristics of Class A amplifiers:

- Unsymmetrical sinking and sourcing
- Linear
- Poor efficiency



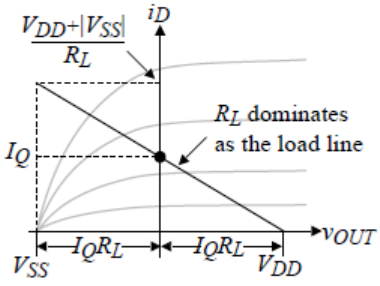


Fig. 5.5-1

$$\text{Efficiency} = \frac{P_{RL}}{P_{Supply}} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})I_Q} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})\left(\frac{(V_{DD}-V_{SS})}{2R_L}\right)} = \left(\frac{v_{OUT}(\text{peak})}{V_{DD}-V_{SS}}\right)^2$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD} = |V_{SS}|$ which gives 25%.

Small-Signal Performance of the Class A Amplifier

Although we have considered the small-signal performance of the Class A amplifier as the current source load inverter, let us include the influence of the load.
The modified small-signal model:

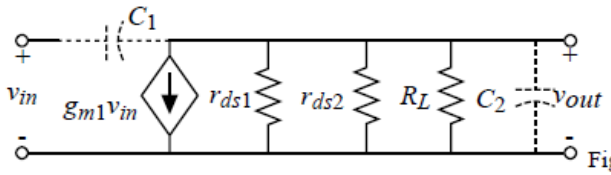


Fig. 5.5-2

The small-signal voltage gain is:

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1}+g_{ds2}+G_L}$$

The small-signal frequency response includes:
A zero at

$$z = \frac{g_{m1}}{C_{gd1}}$$

and a pole at

$$p = \frac{-(g_{ds1}+g_{ds2}+G_L)}{C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}+C_L}$$

Example 5.5-1 - Design of a Simple Class-A Output Stage

Use Table 3.1-2 to design the W/L ratios of M1 and M2 so that a voltage swing of ±2V and a slew rate of ≅1 V/μs is achieved if R_L = 20 kΩ and C_L = 1000 pF. Assume V_{DD} = $|V_{SS}|$ = 3V and V_{GG2} = 0V. Let L = 2 μm and assume that C_{gd1} = 100fF.

Solution

Let us first consider the effects of R_L and C_L.

i_{OUT}(peak) = ±2V/20kΩ = ±100μA and $C_L \cdot SR = 10^{-9} \cdot 10^{6} = 1000\mu A$

Since the slew rate current is so much larger than the current needed to meet the voltage specification across R_L, we can safely assume that all of the current supplied by the inverter is available to charge C_L.
Using a value of ±1 mA,

$$\frac{W_1}{L_1} = \frac{2(I_{OUT^-}+I_Q)}{K_N'(V_{DD}+|V_{SS}|-V_{TN})^2} = \frac{4000}{110\cdot(5.3)^2} \approx \frac{3\mu m}{2\mu m}$$

and

$$\frac{W_2}{L_2} = \frac{2I_{OUT^+}}{K_P'(V_{DD}-V_{GG2}-|V_{TP}|)^2} = \frac{2000}{50\cdot(2.3)^2} \approx \frac{15\mu m}{2\mu m}$$

The small-signal performance is A_v = -8.21 V/V (includes R_L = 20kΩ) and r_{out} = 50kΩ
The roots are, zero = g_{m1}/C_{gd1} ⇒ .59GHz and pole = $1/[(R_L \| r_{out})C_L)]$ ⇒ -11.14kHz

Class-A Source Follower

N-Channel Source Follower with current sink bias:

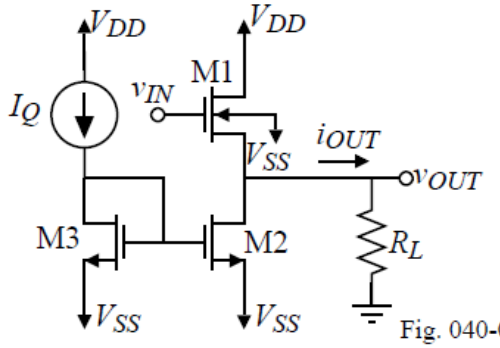


Fig. 040-01

Voltage transfer curve:

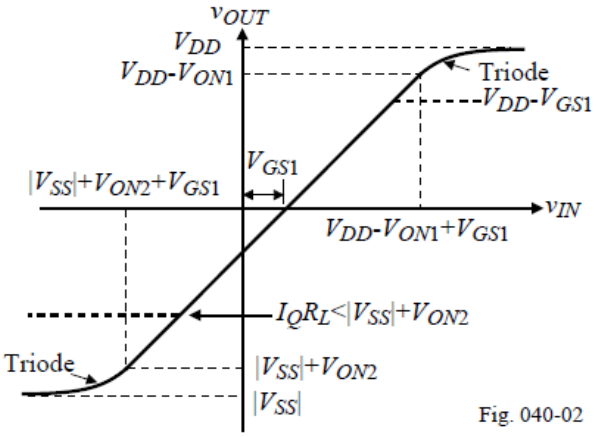


Fig. 040-02

Maximum output voltage swings:

$v_{OUT}(\min) \approx V_{SS} - V_{ON2}$ (if R_L is large) or $v_{OUT}(\min) \approx -I_Q R_L$ (if R_L is small)

$v_{OUT}(\max) = V_{DD} - V_{ON1}$ (if $v_{IN} > V_{DD}$) or $v_{OUT}(\max) \approx V_{DD} - V_{GS1}$

PUSH-PULL AMPLIFIERS

Push-Pull Source Follower

Can both sink and source current and provide a slightly lower output resistance.

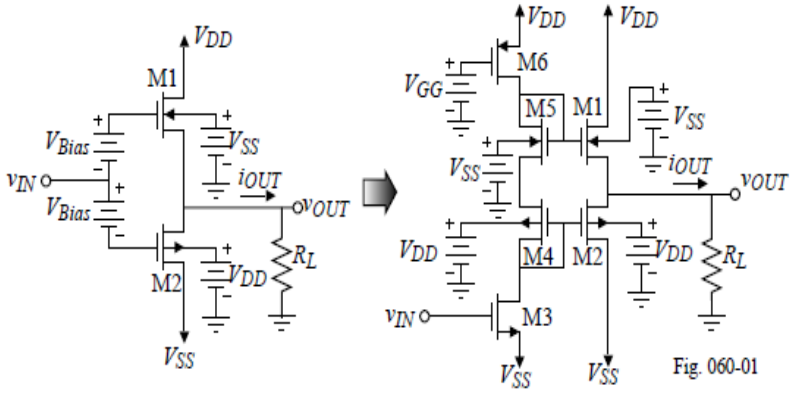


Fig. 060-01

Efficiency:
Depends on how the transistors are biased.

- Class B - one transistor has current flow for only 180° of the sinusoid (half period)

$$\therefore \text{ Efficiency} = \frac{P_{RL}}{P_{VDD}} = \frac{\dfrac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD} - V_{SS})\left(\dfrac{1}{2}\right)\left(\dfrac{2v_{OUT}(\text{peak})}{\pi R_L}\right)} = \frac{\pi}{2}\frac{v_{OUT}(\text{peak})}{V_{DD} - V_{SS}}$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD}$ and is 78.5%

- Class AB - each transistor has current flow for more than 180° of the sinusoid.

Maximum efficiency is between 25% and 78.5%

BIPOLAR JUNCTION TRANSISTOR OUTPUT AMPLIFIERS

What about the use of BJTs?

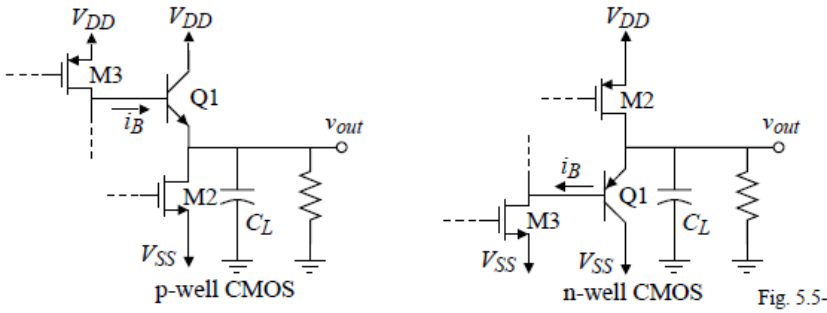


Fig. 5.5-8A

Comments:

- Can use either substrate or lateral BJTs.
- Small-signal output resistance is $1/g_m$ which can easily be less than 100Ω.
- Unfortunately, only PNP or NPN BJTs are available but not both on a standard CMOS technology.
- In order for the BJT to sink (or source) large currents, the base current, i_B, must be large. Providing large currents as the voltage gets to extreme values is difficult for MOSFET circuits to accomplish.
- If one considers the MOSFET driver, the emitter can only pull to within $v_{BE}+V_{ON}$ of the power supply rails. This value can be 1V or more.

We will consider the BJT as an output stage in more detail in Sec. 7.1.

USING NEGATIVE FEEDBACK TO REDUCE THE OUTPUT RESISTANCE

Concept

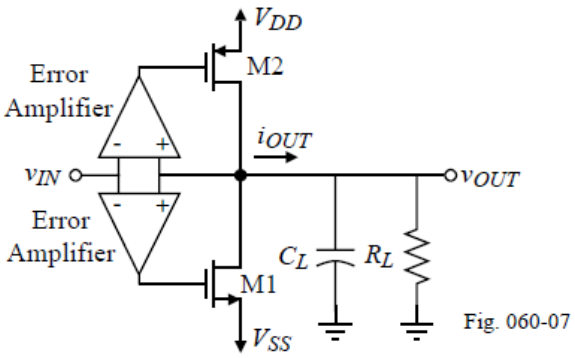


Fig. 060-07

$$R_{out} = \frac{r_{ds1} \| r_{ds2}}{1+\text{Loop Gain}}$$

Comments:

- Can achieve output resistances as low as 10Ω.
- If the error amplifiers are not balanced, it is difficult to control the quiescent current in M1 and M2
- Great linearity because of the strong feedback
- Can be efficient if operated in class B or class AB

Summary of Output Amplifiers

- The objectives are to provide output power in form of voltage and/or current.
- In addition, the output amplifier should be linear and be efficient.
- Low output resistance is required to provide power efficiently to a small load resistance.
- High source/sink currents are required to provide sufficient output voltage rate due to large load capacitances.
- Types of output amplifiers considered:

  Class A amplifier
  Source follower
  Class B and AB amplifier
  Use of BJTs
  Negative shunt feedback

High Gain Amplifiers Architectures:

The philosophy behind the high-gain amplifier is based on the concept of feedback. In analog circuits, we must be able to precisely define transfer functions. A familiar representation of this concept is illustrated by the block diagram of Fig. 5.6-1. In this diagram, x may be a voltage or current, A is the high-gain amplifier, F is the feedback network, and the feedback signal x_f is subtracted from the input signal x_s in the summer. If we assume the signal flow is unidirectional as shown and A and F are independent of the source or load resistance (not shown), then the overall gain of the amplifier can be written as

$$A_f = \frac{x_o}{x_s} \approx \frac{A}{1 + AF}$$

In order to precisely define A_f we need only define F if A is sufficiently large. Typically, F is implemented with passive components such as resistors or capacitors.

The high-gain amplifier is defined in terms of $A = \frac{x_o}{x_i}$

Because x can be voltage or current there are four different types of high-gain amplifiers that will be examined in this section.

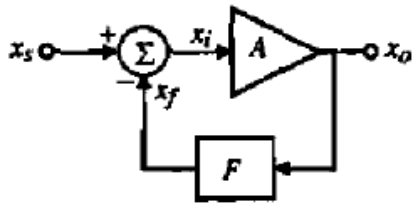


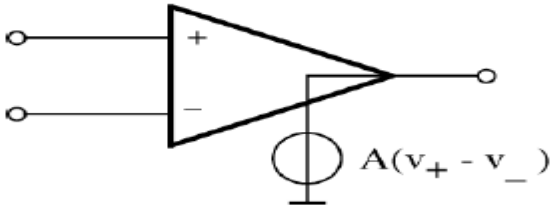
Figure 5.6-1 A general, single-loop, negative feedback circuit.

UNIT -IV:
CMOS Operational Amplifiers

Design of CMOS Op Amps:

Basic op-amp

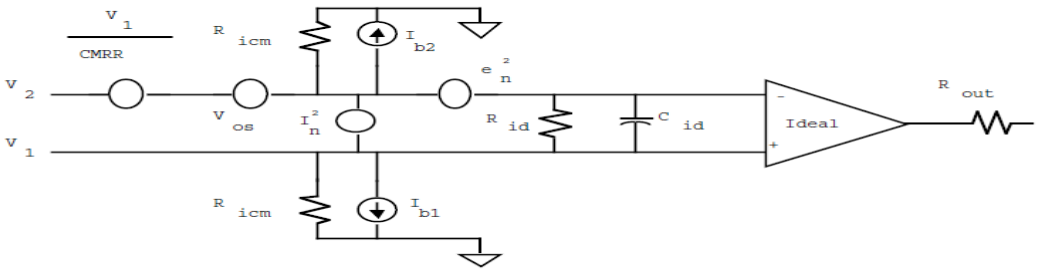
The ideal operational amplifier is a voltage controlled voltage source with infinite gain, infinite input impedance and zero output impedance.



The op-amp is always used in feedback configuration.

Op Amp Characteristics

Non-ideal model for an op amp



Boundary Conditions	Requirement
Process Specification	See Tables 3.1-1 and 3.1-2
Supply Voltage	+5 V ±10%
Supply Current	100 μA
Temperature Range	0 to 70°C
Typical Specifications	
Gain	≥ 80 dB
Gainbandwidth	≥ 10 MHz
Settling Time	≤ 0.1 μsec
Slew Rate	≥ 2 V/μsec
Input CMR	≥ ±2 V
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Output Swing	≥ 2 VP-P
Output Resistance	Capacitive load only
Offset	≤ ±5 mV
Noise	≤ 50nV/$\sqrt{Hz}$ at 1KHz
Layout Area	≤ 10,000 square μm

Power supply rejection ratio (PSRR):

$$\text{PSRR} = \left(\frac{\Delta V_{DD}}{\Delta v_{OUT}}\right) \cdot A_{vd}(s) = \frac{A_{vd}(s)}{A_{ps}(s)} = \frac{\frac{v_{out}}{v_{in}}(v_{ps}=0)}{\frac{v_{out}}{v_{ps}}(v_{in}=0)}$$

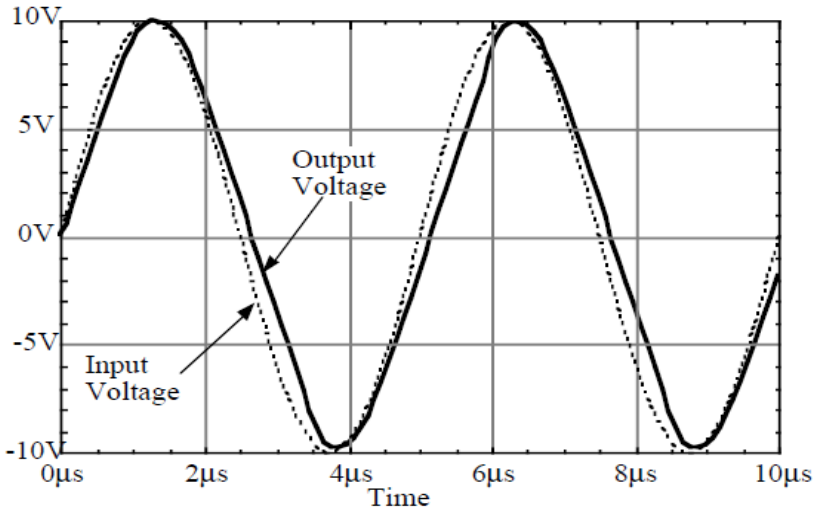
Common-mode input range (ICMR).

Maximum common mode signal range over which the differential voltage gain of the op amp remains constant.

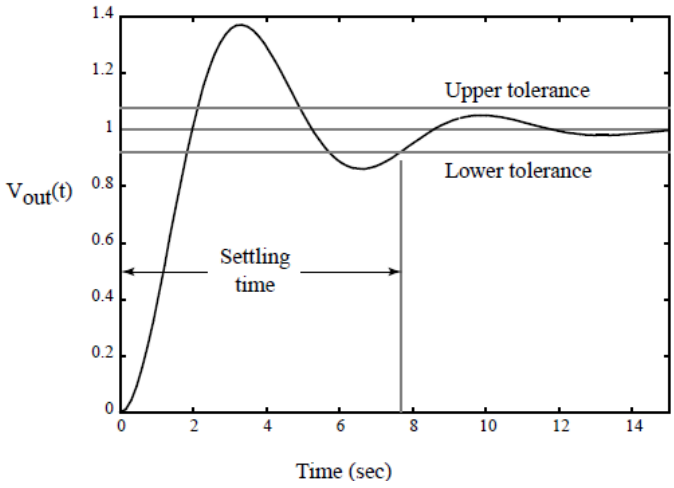
Maximum and minimum output voltage swing.

Slew rate:

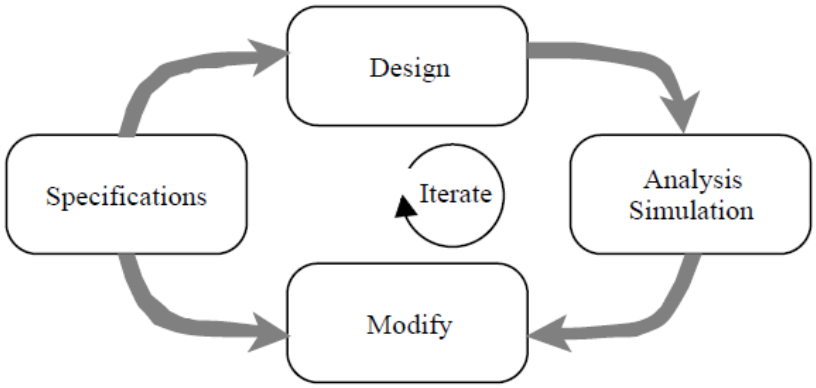
$$\text{Slew rate} = \max\left(\frac{\Delta v_{OUT}}{\Delta t}\right)$$



Settling Time



Design Approach



Specifications:

- Gain
- Output voltage swing
- Settling time
- Power dissipation
- Supply voltage
- Silicon area
- Bandwidth
- PSRR
- CMRR
- Noise
- Common-mode input range

Design Strategy

The design process involves two distinct activities:

Architecture Design

- Find an architecture already available and adapt it to present requirements
- Create a new architecture that can meet requirements

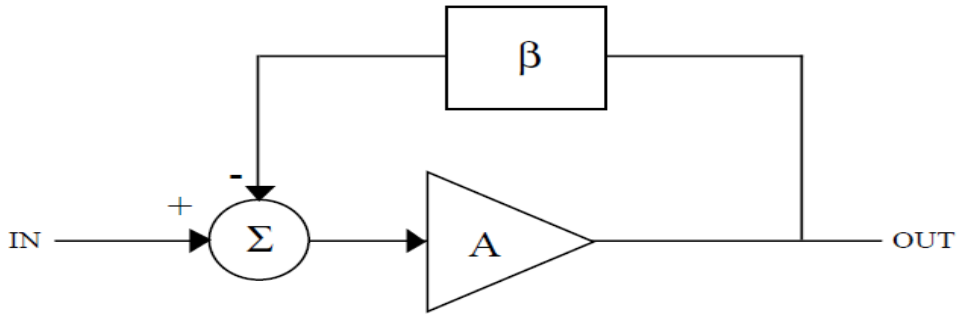
Component Design

- Design transistor sizes
- Design compensation network

If available architectures do not meet requirements, then an existing architecture must be modified, or a new one designed. Once a satisfactory architecture has been obtained, then devices and the compensation network must be designed.

Compensation of Op Amps:

In virtually all op amp applications, feedback will be applied around the amplifier. Therefore, stable performance requires that the amplifier be compensated. Essentially we desire that the loop gain be less than unity when the phase shift around the loop is greater than 135°

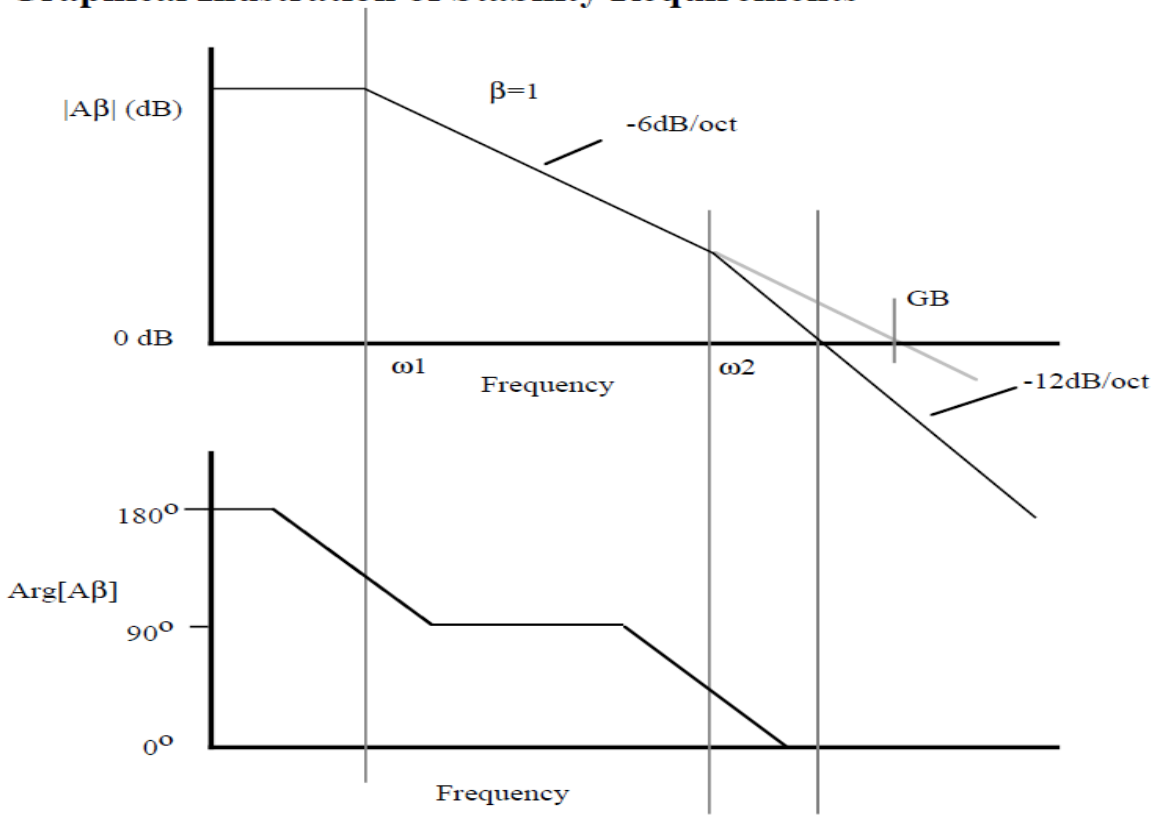


$$\frac{OUT}{IN} = \frac{A}{1 + A\beta}$$

Goal: $1 + A\beta > 0$

Rule of thumb: $\arg[A\beta] < 135^\circ$ at $\text{mag}[A\beta] = 1$

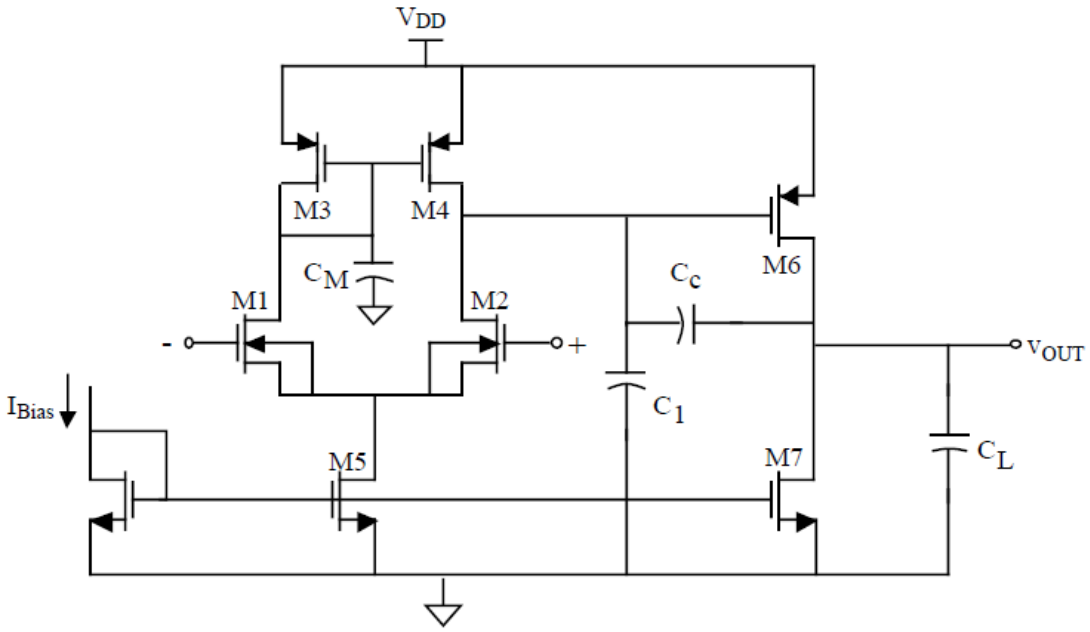
Graphical Illustration of Stability Requirements



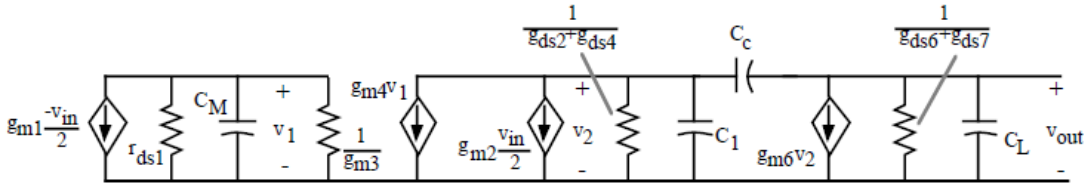
Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
    - Miller capacitor only
    - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
    - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Self compensating - Load capacitor compensates the op amp (later).
3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

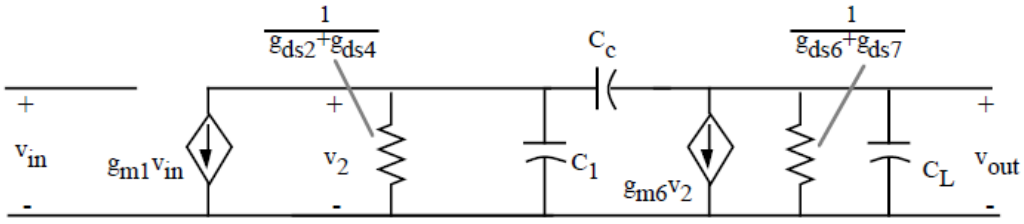
Miller Compensation



Small-signal model



Simplified small-signal model



Analysis

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})(1 - sC_c/g_{mII})}{1 + s[R_I(C_1 + C_c) + R_{II}(C_L + C_c) + g_{mII}R_IR_{II}C_c] + s^2R_IR_{II}[C_1C_L + C_c(C_1 + C_L)]}$$

$$p_1 \cong \frac{-1}{g_{mII} R_I R_{II} C_c}$$

$$p_2 \cong \frac{-g_{mII} C_c}{C_1 C_L + C_L C_c + C_1 C_c}$$

$$p_2 \cong \frac{-g_{mII}}{C_L}$$

$$z_1 = \frac{g_{mII}}{C_c}$$

where

$$g_{mI} = g_{m1} = g_{m2} \qquad g_{mII} = g_{m6}$$

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} \qquad R_{II} = \frac{1}{g_{ds6} + g_{ds7}}$$

Conditions for Stability

- Unity-gainbandwith is given as:

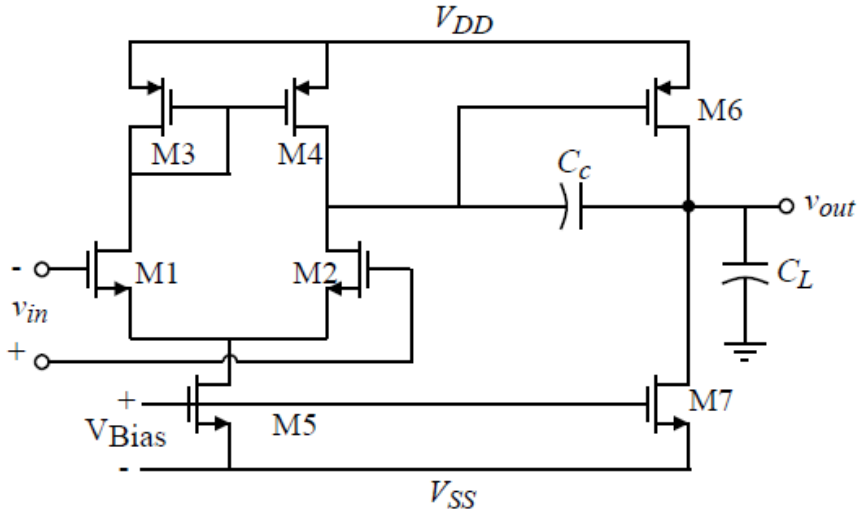
$$GB = A_v(0) \cdot |p_1| = (g_{mI} g_{mII} R_I R_{II}) \cdot \left(\frac{1}{g_{mII} R_I R_{II} C_c} \right) = \frac{g_{mI}}{C_c}$$

- The requirement for 45° phase margin is:

$$\text{Arg}[A\beta] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Design of Two Stage Op Amps:

Two-Stage Operational Amplifier Design



Important relationships:

$g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$.

Slew rate $SR = \frac{I_5}{C_c}$ (1)

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$ (2)

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$ (3)

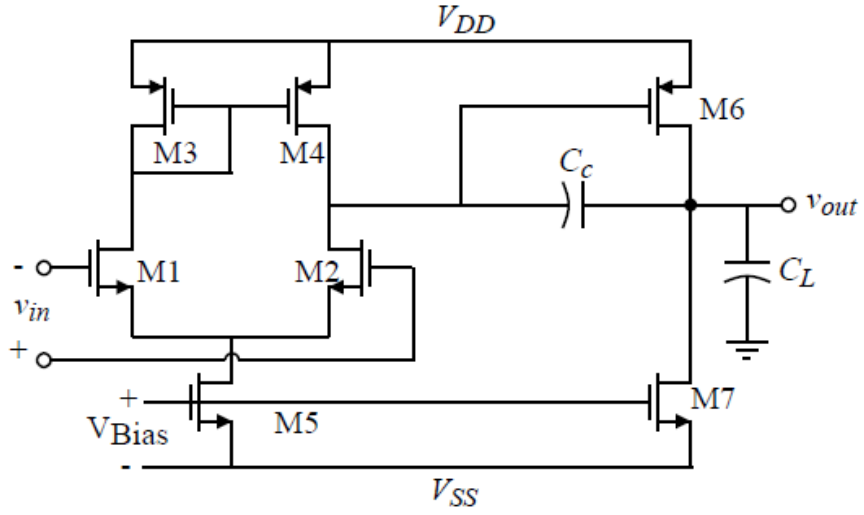
Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$ (4)

Output pole $p_2 = \frac{-g_{m6}}{C_L}$ (5)

RHP zero $z_1 = \frac{g_{m6}}{C_c}$ (6)

Positive CMR $V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{(\max)} + V_{T1(\min)})$ (7)

Two-Stage Operational Amplifier Design



Important relationships:

$g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$.

Slew rate $SR = \dfrac{I_5}{C_c}$ (1)

First-stage gain $A_{v1} = \dfrac{g_{m1}}{g_{ds2} + g_{ds4}} = \dfrac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$ (2)

Second-stage gain $A_{v2} = \dfrac{g_{m6}}{g_{ds6} + g_{ds7}} = \dfrac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$ (3)

Gain-bandwidth $GB = \dfrac{g_{m1}}{C_c}$ (4)

Output pole $p_2 = \dfrac{-g_{m6}}{C_L}$ (5)

RHP zero $z_1 = \dfrac{g_{m6}}{C_c}$ (6)

Positive CMR $V_{\text{in(max)}} = V_{DD} - \sqrt{\dfrac{I_5}{\beta_3}} - |V_{T03}|_{(\max)} + V_{T1(\min)})$ (7)

$$\text{Negative CMR } V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\max)} + V_{DS5}(\text{sat}) \tag{8}$$

$$\text{Saturation voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \tag{9}$$

All transistors are in saturation for the above relationships.

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Input common-mode range, ICMR
4. Load Capacitance, C_L
5. Slew-rate, SR
6. Output voltage swing
7. Power dissipation, P_{diss}

Choose a device length to establish of the channel-length modulation parameter λ.

Design the compensation capacitor C_c. It was shown that placing the loading pole p_2 2.2 times higher than the GB permitted a 60° phase margin (assuming that the RHP zero z_1 is placed at or beyond ten times GB). This results in the following requirement for the minimum value for C_c.

$$C_c > (2.2/10)C_L$$

Next, determine the minimum value for the tail current I_5, based upon slew-rate requirements. Using Eq. (1), the value for I_5 is determined to be

$$I_5 = SR\ (C_c)$$

If the slew-rate specification is not given, then one can choose a value based upon settling-time requirements. Determine a value that is roughly ten times faster than the settling-time specification, assuming that the output slews approximately one-half of the supply rail. The value of I_5 resulting from this calculation can be changed later if need be.

The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ was derived from Eq. (7).

$$S_3 = (W/L)_3 = \frac{I_5}{(K'_3)\,[V_{DD} - V_{\text{in}}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$$

If the value determined for $(W/L)_3$ is less than one, then it should be increased to a value that minimizes the product of W and L. This minimizes the area of the gate region, which

in turn reduces the gate capacitance. This gate capacitance will affect a pole-zero pair which causes a small degradation in phase margin.

Requirements for the transconductance of the input transistors can be determined from knowledge of C_c and GB. The transconductance g_{m2} can be calculated using the following equation

$$g_{m1} = GB(C_c)$$

The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below

$$S_1 = (W/L)_1 = \frac{g_{m1}^2}{(K'_2)(I_5)}$$

Enough information is now available to calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate V_{DS5} using the following relationship derived from Eq. (8).

$$V_{DS5} = V_{\text{in}}(\min) - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{1/2} - V_{T1}(\max)$$

If the value for V_{DS5} is less than about 100 mV then the possibility of a rather large $(W/L)_5$ may result. This may not be acceptable. If the value for V_{DS5} is less than zero, then the ICMR specification may be too stringent. To solve this problem, I_5 can be reduced or $(W/L)_1$ increased. The effects of these changes must be accounted for in previous design steps. One must iterate until the desired result is achieved. With V_{DS5} determined, $(W/L)_5$ can be extracted using Eq. (9) in the following way

$$S_5 = (W/L)_5 = \frac{2(I_5)}{K'_5(V_{DS5})^2}$$

For a phase margin of 60°, the location of the loading pole was assumed to be placed at 2.2 times GB. Based upon this assumption and the relationship for $|p_2|$ in Eq. (5), the transconductance g_{m6} can be determined using the following relationship

$$g_{m6} = 2.2(g_{m2})(C_L/C_c)$$

Since S_3 is known as well as g_{m6} and g_{m3}, assuming balanced conditions,

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

I_6 can be calculated from the consideration of the "proper mirroring" of first-stage the current mirror load of Fig. 6.3-1. For accurate current mirroring, we want V_{SD3} to be equal to V_{SD4}. This will occur if V_{SG4} is equal to V_{SG6}. V_{SG4} will be equal to V_{SG6} if

$$I_6 = \frac{(W/L)_6}{(W/L)_4} I_1 = \left(\frac{S_6}{S_4}\right) I_1$$

Choose the larger of these two values for I_6 (Eq. 19 or Eq. 20). If the larger value is found in Eq (19), then $(W/L)_6$ must be increased to satisfy Eq. (20). If the larger value is found in Eq. (20), then no other adjustments must be made. One also should check the power dissipation requirements since I_6 will most likely determine the majority of the power dissipation.

The device size of M7 can be determined from the balance equation given below

$$S_7 = (W/L)_7 = (W/L)_5 \left(\frac{I_6}{I_5}\right) = S_5 \left(\frac{I_6}{I_5}\right)$$

The first-cut design of all W/L ratios are now complete. Fig. 6.3-2 illustrates the above design procedure showing the various design relationships and where they apply in the two-stage CMOS op amp.

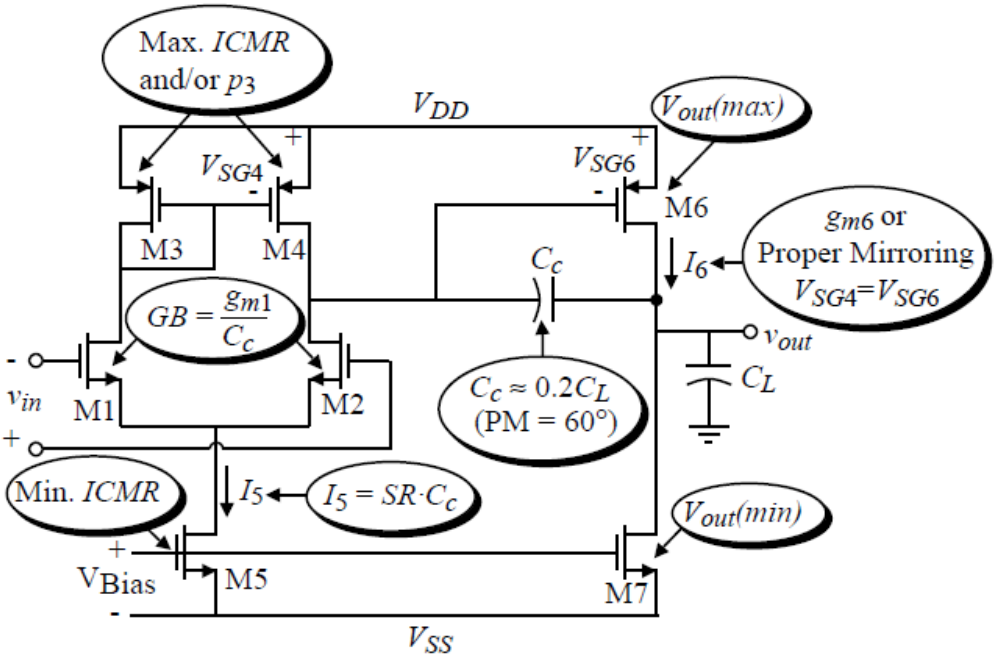


Figure 6.3-2 Illustration of the design relationships and the circuit for a two-stage CMOS op amp.

At this point in the design procedure, the total amplifier gain must be checked against the specifications.

$$A_v = \frac{(2)(g_{m2})(g_{m6})}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

If the gain is too low, a number of things can be adjusted. The best way to do this is to use the table below, which shows the effects of various device sizes and currents on the

different parameters generally specified. Each adjustment may require another pass through this design procedure in order to insure that all specifications have been met. Table 6.3-2 summarizes the above design procedure.

Dependencies of device performance on various parameters

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Comp. Cap..
	I_5	I_7	W/L	L	W	L	W_6/L_6	W_7	L_7	C_c
Increase DC Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase GB	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$							$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$					$(\uparrow)^{1/2}$			$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\downarrow$

Design Procedure:

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given.

1. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.
2. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22 C_L$$

3. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

$$I_5 = SR \cdot C_c$$

$$I_5 \equiv 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

4. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \geq 1$$

5. Verify that the pole of M3 due to C_{gs3} and C_{gs4} (=$0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 *GB*

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

6. Design for S_1 (S_2) to achieve the desired *GB*.

$$g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}^2}{K'_2 I_5}$$

7. Design for S_5 from the minimum input voltage. First calculate V_{DS5}(sat) then find S_5.

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV}$$

$$S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

8. Find g_{m6} and S_6 by the relationship relating to phase margin, load, and compensat capacitors, and the balance condition.

$$g_{m6} = 2.2g_{m2}(C_L/C_c)$$

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

9. Calculate I_6 :

$$I_6 = (S_6/S_4)I_4 = (S_6/S_4)(I_5/2)$$

10. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = (I_6/I_5)S_5$$

11. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

12. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they have been satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.
13. Simulate the circuit to check to see that all specifications are met.

Example: Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1μm.

$A_v > 3000$V/V	$V_{DD} = 2.5$V	$V_{SS} = -2.5$V
$GB = 5$MHz	$C_L = 10$pF	$SR > 10$V/μs
V_{out} range = ±2V	$ICMR = -1$ to 2V	$P_{diss} \le 2$mW

Solution

Calculate the minimum value of the compensation capacitor C_c

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3 \times 10^{-12})(10 \times 10^6) = 30\ \mu\text{A}$$

Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(50 \times 10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 15$$

$$g_{m3} = \sqrt{2 \times 50\text{x}10^{-6}\ \text{x}15\text{x}10^{-6} \times 15} = 150\mu\text{S}$$

Therefore

$$(W/L)_3 = (W/L)_4 = 15$$

Check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 0.4\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = 15.75\text{x}10^9(\text{rads/sec})$$

or 2.98 GHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

The next step in the design is to calculate g_{m1}

$$g_{m1} = (5 \times 10^6)(2\pi)(3 \times 10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{{g_{m1}}^2}{2K'_N I_1} = \frac{(94.25)^2}{2 \cdot 110 \cdot 15} = 2.79 \approx 3.0$$

Next calculate V_{DS5}

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30 \times 10^{-6}}{110 \times 10^{-6} \cdot 3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from Eq. (16)

$$(W/L)_5 = \frac{2(30 \times 10\text{-}6)}{(50 \times 10\text{-}6)(0.35)^2} = 4.49 \approx 4.5$$

From Eq. (20) of Sec. 6.2, we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$

$$(W/L)_6 = 15 \ \frac{942.5 \times 10\text{-}6}{150 \times 10\text{-}6} = 94.25$$

Using the equations for proper mirroring, I_6 is determined to be

$$I_6 = (15 \times 10\text{-}6)(94.25/15) = 94.25\ \mu\text{A}$$

Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5\left(\frac{94.25 \times 10\text{-}6}{30 \times 10\text{-}6}\right) \approx 14.14$$

Check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{min}(\text{out}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \times 94.25}{110 \times 14.14}} = 0.348\text{V}$$

which is much less than required. At this point, the first-cut design is complete. Examining the results shows that the large value of M7 is due to the large value of M5 which in turn is due to a tight specification on the negative input common mode range. To reduce these values the specification should be loosened or a different architecture (i.e. p-channel input pair) examined.

Now check to see that the gain specification has been met

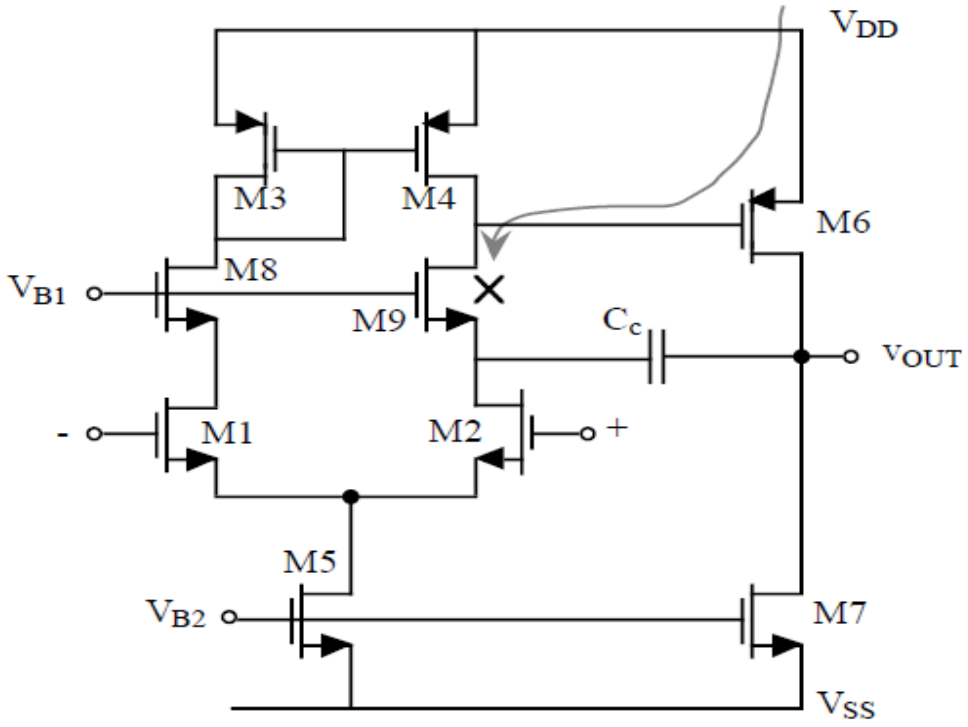
$$A_v = \frac{(2)(94.25 \times 10\text{-}6)(942.5 \times 10\text{-}6)}{30 \times 10\text{-}6(.04 + .05)38 \times 10\text{-}6(.04 + .05)} = 19{,}240$$

which meets specifications.

Power-Supply Rejection Ratio of Two-Stage Op Amps:

Improved PSRR For Two-Stage OTA

Use cascode to reject C_c feedforward



+PSRR is reduced by M9

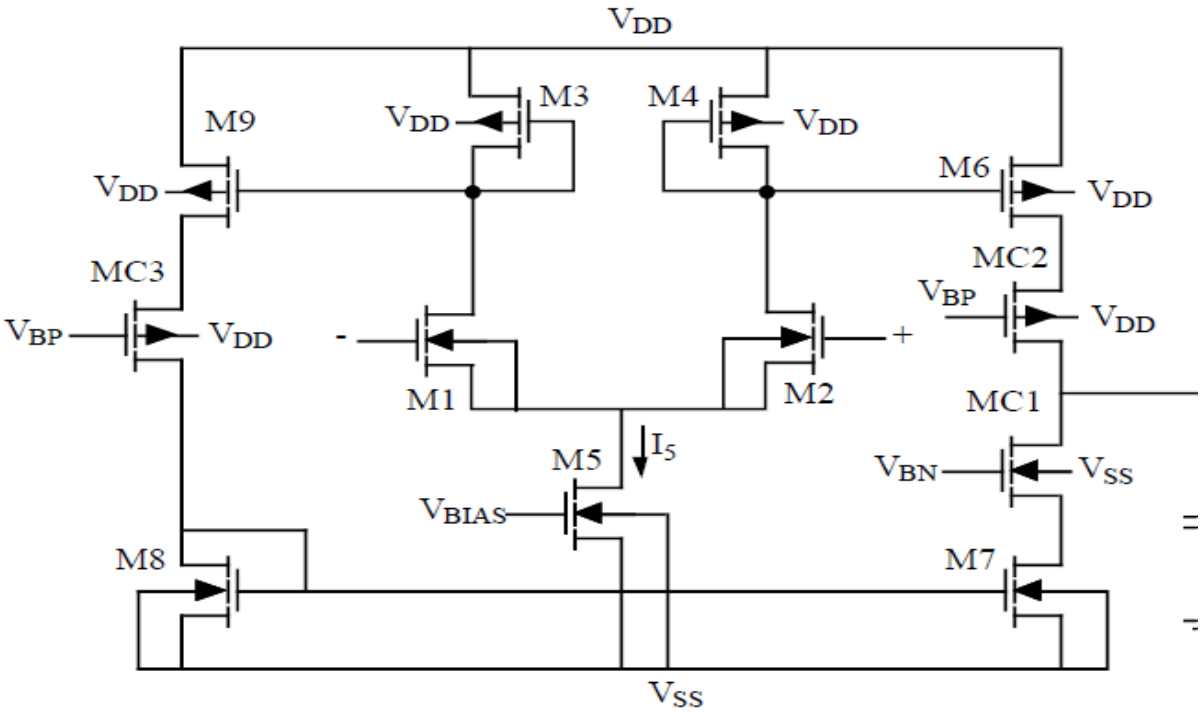
Disadvantage -

Miller pole is larger because $R_1 \approx \frac{1}{g_{m9}}$

positive input common mode range is restricted

Cascode Op Amps:.

LOAD COMPENSATED CASCODE AMPLIFIER



$$\left.\begin{aligned} A_{V1} &= \frac{g_{m2}}{g_{m4}} \\ A_{V2} &= \frac{1}{2}(g_{m6} + g_{m9})R_o \end{aligned}\right\} \quad A_V = \frac{g_{m2}}{2(g_{m4})}(g_{m6} + g_{m9})\, R_o$$

where

$$R_o \approx (g_{mc2}r_{dsc2})r_{ds6} \parallel (g_{mc1}r_{dsc1})r_{ds7} \text{ and } M7 = M8$$

Or,

$$A_V = \left(\frac{g_{m1}+g_{m2}}{2}\right) KR_o$$

where

$$K = \frac{W_6/L_6}{W_4/L_4} = \frac{W_9/L_9}{W_3/L_3}$$

Design Example

Pertinent design equations:

$$SR = \frac{i_{OUT}}{C_L}$$

$$A_V = \frac{g_{m2}}{2(g_{m4})}(g_{m6} + g_{m7})\, r_o$$

$$GB = \frac{g_{m2}(g_{m6} + g_{m7})}{2(g_{m4})C_L}$$

$$V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T3}|(max) + V_{T1}(min)$$

$$V_{in(min)} = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(max)$$

Specifications:

$V_{DD} = -V_{SS} = 5V$

SR = 5V/μs into C_L = 50pf

GB = 5 MHz

$A_V > 5000$

CMR = ±3V

Output swing = ±3V

Measurement Techniques of OP Amp.:

In designing a CMOS op amp, the designer starts with building blocks whose performance can be analyzed to a first-order approximation by hand/calculator methods of analysis. The advantage of this step is the insight it provides to the designer as the design of the circuit develops. However, at some point the designer must turn to a better means of simulation. For the CMOS op amp this is generally a computer-analysis program such as SPICE. With the insight of the first-order analysis and the modeling capability of SPICE, the circuit design can be optimized and many other questions (such as tolerances, stability, and noise) can be examined.

Fabrication follows the simulation and layout of the MOS op amp. After fabrication the MOS op amp must be tested and evaluated. The techniques for testing various parameters of the op amp can be as complex as the design of the op amp itself. Each specification must be verified over a large number of op amps to ensure a working op amp in case of process variations.

The categories of op amp measurements and simulations discussed include: open-loop gain, open-loop frequency response (including the phase margin), input-offset voltage, common-mode gain, power-supply rejection ratio, common-mode input- and output-voltage ranges, open-loop output resistance, and transient response including slew rate. Configurations and techniques for each of these measurements will be presented in this section.

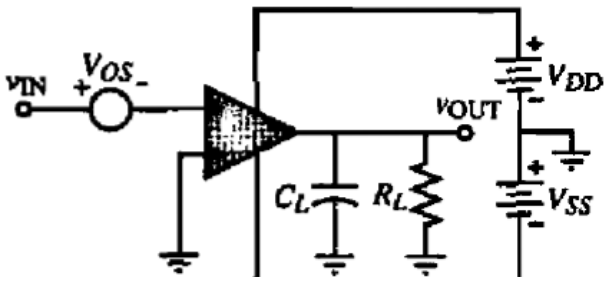
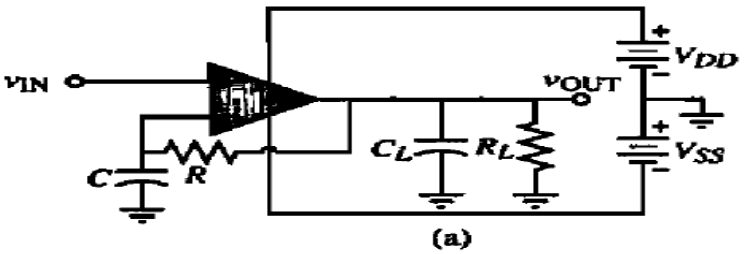
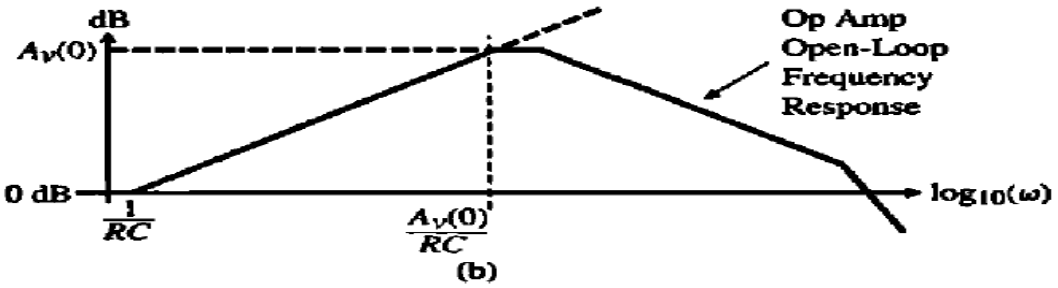


Figure 6.6-1 Open-loop mode with offset compensation.



(a)



(b)

Figure 6.6-2 (a) A method of measuring the open-loop characteristics with dc bias stability. (b) Asymptotic magnitude plot of the voltage-transfer function.

UNIT -V
Comparators

Characterization of Comparator:

What is a Comparator?

A comparator is a circuit which compares two analog signals and outputs a binary signal based on the comparsion. (It can be an op amp without frequency compensation.)

Characterization of Comparators

We shall characterize the comparator by the following aspects:

- Resolving capability
- Speed or propagation time delay
- Maximum signal swing limits
- Input offset voltage
- Other Considerations

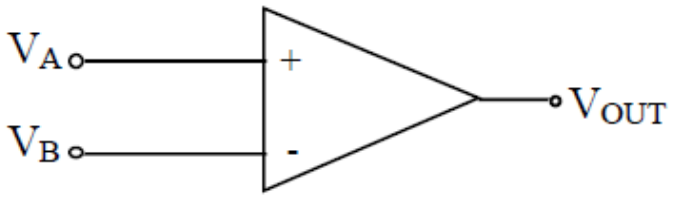
  Noise

  Power

  Etc.

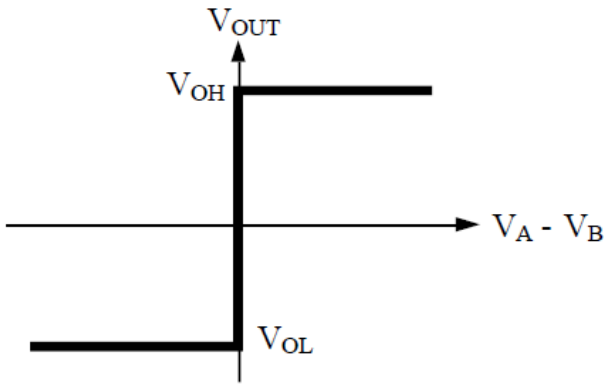
VOLTAGE COMPARATORS

Definition of a Comparator



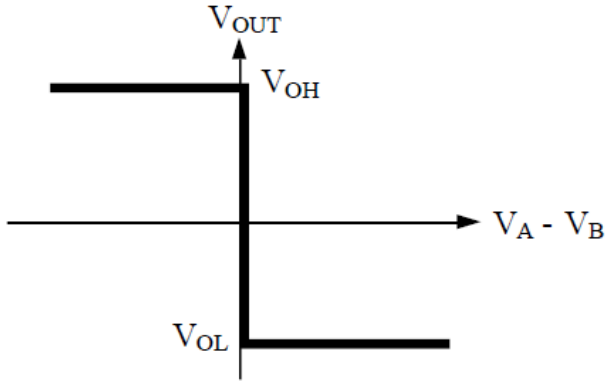
Noninverting

$$V_{OUT} = \begin{cases} V_{OH} & \text{when } V_A \geq V_B \\ V_{OL} & \text{when } V_A < V_B \end{cases}$$



Inverting

$$V_{OUT} = \begin{cases} V_{OL} & \text{when } V_A \geq V_B \\ V_{OH} & \text{when } V_A \leq V_B \end{cases}$$



COMPARATOR PERFORMANCE

1. Speed or propagation time delay.
   The amount of time between the time when $V_A - V_B = 0$ and the output is 50% between initial and final value.

2. Resolving capability.
   The input change necessary to cause the output to make a transition between its two stable states.

3. Input common mode range.
   The input voltage range over which the comparator can detect $V_A = V_B$.

4. Output voltage swing (typically binary).

5. Input offset voltage.
   The value of V_{OUT} reflected back to the input when V_A is physically connected to V_B.

APPROACHES TO THE DESIGN OF VOLTAGE COMPARATORS

Open Loop

Use of a high-gain differential amplifier.

$$\text{Gain} = \frac{V_{OH} - V_{OL}}{\text{resolution of the comparator}}$$

Regenerative

Use of positive feedback to detect small differences between two voltages, V_A and V_B. I.e., sense amplifiers in digital memories.

Open Loop - Regenerative

Use of low gain, high speed comparator cascaded with a latch. Results in comparators with very low propagation time delay.

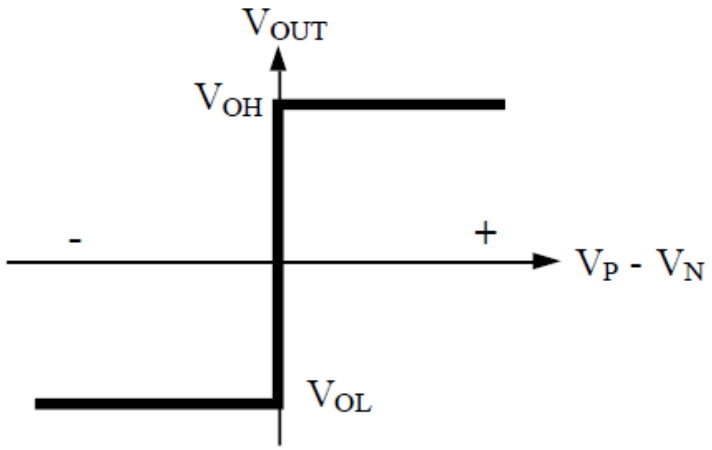
Charge Balancing

Differential charging of a capacitor. Compatible with switched capacitor circuit techniques.

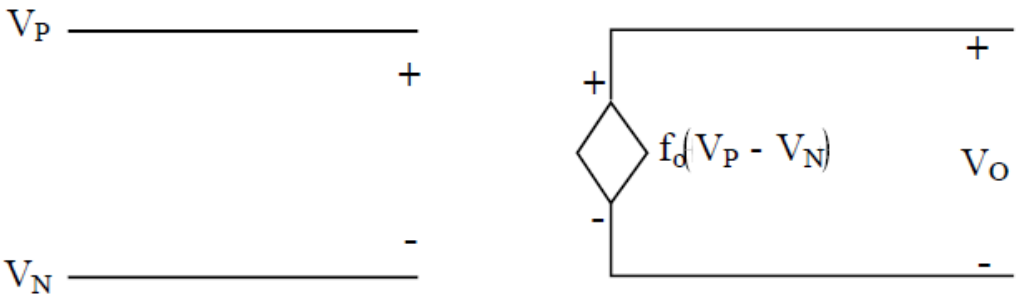
Type	Offset Voltage (Power supply)	Resolution	Speed (8 bit)
Open-loop	1-10 mV	300µV (±5V)	10 MHz
Regenerative	0.1 mV	50µV (±5V)	50 MHz
Charge Balancing	0.1 mV	5mV (5V)	30 MHz

COMPARATOR MODELS - OPEN LOOP

Zero Order Model



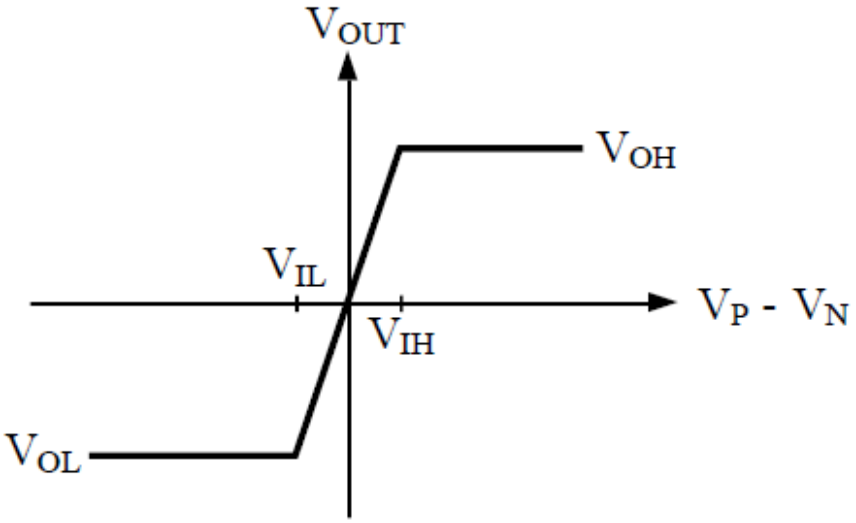
Model



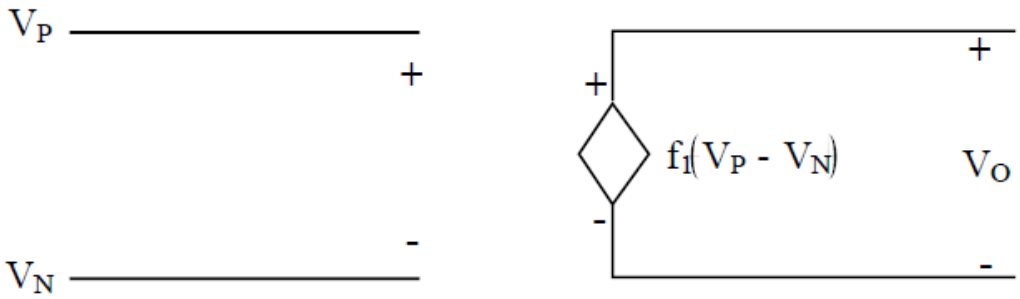
$$f_{o(V_P - V_N)} = \begin{cases} V_{OH} & \text{for } (V_P - V_N) \geq 0 \\ V_{OL} & \text{for } (V_P - V_N) \leq 0 \end{cases}$$

First Order Model

Transfer Curve



Model

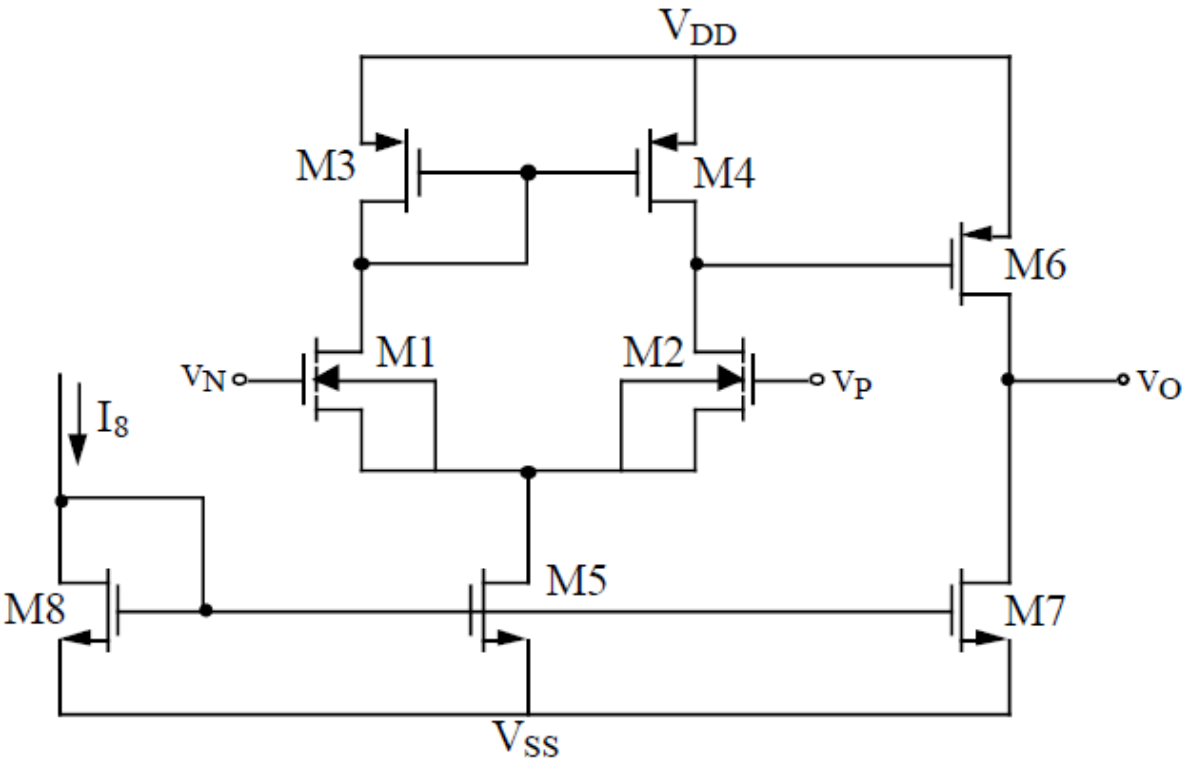


$$f_{1(V_P - V_N)} = \begin{cases} V_{OH} \quad \text{for } (V_P - V_N) \geq V_{IH} \\ A_{V(V_P - V_N)} \quad \text{for } V_{IL} \leq (V_P - V_N) \leq V_{IH} \\ V_{OL} \quad \text{for } (V_P - V_N) \leq V_{IL} \end{cases}$$

TWO-STAGE COMPARATOR

Combine the differential amplifier stage with the inverter stage.

- Sufficient gain.
- Good signal swing.



Design of Two stage Comparator:

DC BALANCE CONDITIONS FOR TWO-STAGE COMPARATOR

- Try to keep all devices in saturation - more gain and wider signal swings.

- Based on gate-source and DC current relationship. I.e. if M1 and M2 are two matched devices and if $V_{GS1} = V_{GS2}$, then $I_{D1} = I_{D2}$ or vice versa.

Let $S_1 = \frac{W_1}{L_1}$,

M1 and M2 matched gives $S_1 = S_2$.

M3 and M4 matched gives $S_3 = S_4$.

also, $I_1 = I_2 = 0.5I_5$.

From gate-source matching, we have

$V_{GS5} = V_{GS7}$ ' $I_7 = I_5\left(\frac{S_7}{S_5}\right)$ and $I_6 = I_4\left(\frac{S_6}{S_4}\right)$ ← Assume $V_{GS4} = V_{GS6}$

For balance conditions, I_6 must be equal to I_7, thus

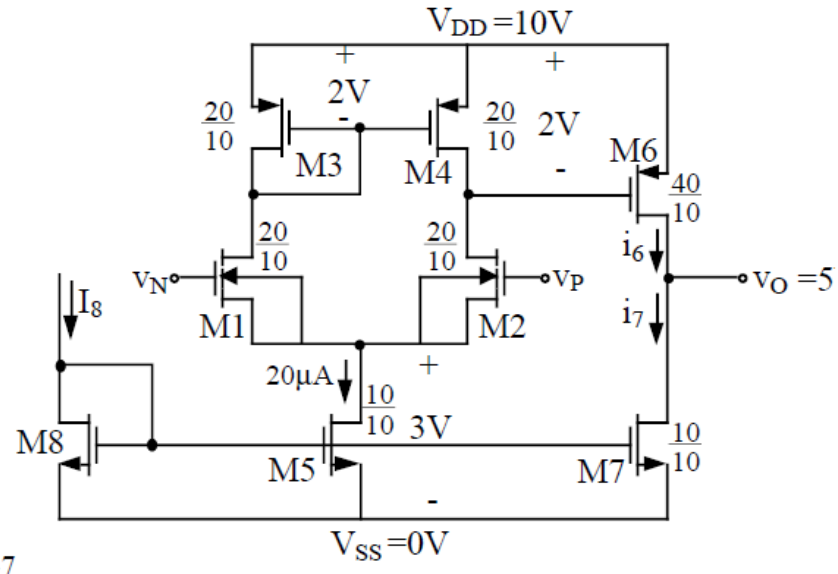
$$\frac{I_5}{I_4} \cdot \frac{S_7}{S_5} = \frac{S_6}{S_4}$$

Since $\frac{I_5}{I_4} = 2$, then DC balance is achieved under the following:

$$\boxed{\frac{S_6}{S_4} = 2 \cdot \frac{S_7}{S_5}}$$ ' $V_{DG4} = 0$ ' M4 is saturated.

SYSTEMATIC OFFSET ERROR

$K_N = 24.75\ \mu A/V^2$
$K_P = 10.125\ \mu A/V^2$
$V_{TN} = -V_{TP} = 1V$
$\lambda_N = 0.015V^{-1}$
$\lambda_P = 0.020V^{-1}$



Find V_{OS} to make $i_6 = i_7$

(1) Find the mismatch between i_6 and i_7

$$\frac{i_7}{i_5} = \left(\frac{1 + \lambda_N v_{DS7}}{1 + \lambda_N v_{DS5}}\right)\left(\frac{W_7/L_7}{W_5/L_5}\right) = \frac{1 + (0.015)(5)}{1 + (0.015)(3)}(1) = 1.029$$

$$\frac{i_6}{i_4} = \left(\frac{1 + \lambda_P v_{DS6}}{1 + \lambda_P v_{DS4}}\right)\left(\frac{W_6/L_6}{W_4/L_4}\right) = \frac{1 + (0.02)(5)}{1 + (0.02)(2)}(2) = 2.115$$

$i_5 = 2i_4$

$\therefore\ i_7 = (1.029)(2)i_4 = 2.057i_4$ and $i_6 = 2.115i_4$

(2) Find how much v_{GS6} must be reduced to make $i_6 = i_7$

$$\Delta v_{GS6} = v_{GS6}(2.115i_4) - v_{GS6}(2.057i_4)$$

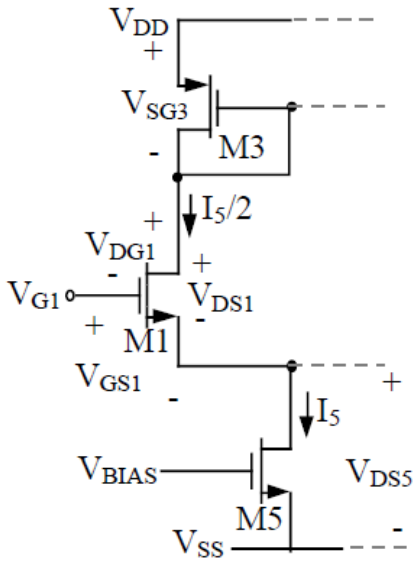
$$\Delta v_{GS6} = \sqrt{\frac{2L_6}{K_P W_6}\, i_4}\left(\sqrt{2.115} - \sqrt{2.057}\right) = 14.11\ mV$$

(3) Reflecting Δv_{GS6} into the input

$$A_v(diff) = \left(\frac{2}{\lambda_2 + \lambda_4}\right)\sqrt{\frac{K_N(W_2/L_2)}{I_5}} = 89.9$$

$$\therefore\ V_{OS} = \frac{\Delta v_{GS6}}{A_v(diff)} = \frac{14.1\ mV}{89.9} = \underline{0.157\ mV}$$

DESIGNING FOR COMMON MODE INPUT RANGE



$$v_{G1}(\min) = V_{SS} + V_{DS5} + V_{GS1}$$

$$\boxed{v_{G1}(\min) = V_{SS} + V_{DS5} + V_{T1}(\max) + \sqrt{\frac{I_5}{2\beta_1}}}$$

$$v_{G1}(\max) = V_{DD} - V_{SG3} - V_{DG1}(\text{sat})$$

$$\boxed{v_{G1}(\max) = V_{DD} - \sqrt{\frac{I_5}{2\beta_3}} - \left|V_{T3}(\max)\right| + V_{T1}(\text{m}}$$

where $V_{DG1}(\text{sat}) = -V_{T1}$

Example

Design M1 through M4 for a CM input range 1.5 to 9 Volts when V_{DD} = 10 V, I_{SS} = 40μA, and V_{SS} = 0V. Table 3.1-2 parameters with $|V_{TN,P}|$ = 0.4 to 1.0 Volts,

$$v_{G1}(\min) = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max)$$

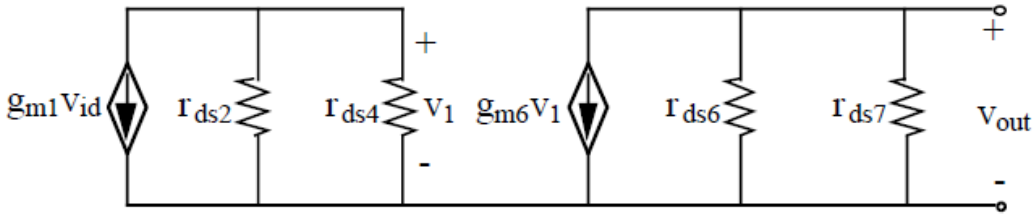
$$1.5 = 0 + 0.1 + \sqrt{\frac{40\mu A}{\beta_1}} + 1$$ (assumed $V_{DS5} \approx 0.1$V- it probably more reasonable to assume β_1 is already defined and find β_5)

$$\beta_1 = \frac{K_N W_1}{L_1} = 250\ \mu A/V^2 \cdot \quad \boxed{\frac{W_1}{L_1} = \frac{W_2}{L_2} = 14.70}$$

$$v_{G1}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T3}(\max)| + V_{T1}(\min)$$

$$\beta_3 = \frac{K_P W_3}{L_3} = 250\ \mu A/V^2 \cdot \quad \boxed{\frac{W_3}{L_3} = \frac{W_4}{L_4} = 31.25}$$

GAIN OF THE TWO-STAGE COMPARATOR



$v_{id} = v_P - v_N$

$$A_V = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right)$$

$$A_V = \frac{2\sqrt{K_N K_P\left(\frac{W_1}{L_1}\right)\left(\frac{W_6}{L_6}\right)}}{(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)\sqrt{I_1 I_6}}$$

Using $\frac{W_1}{L_1} = 5$, $\frac{W_6}{L_6} = 5$, $\lambda_N = 0.015V^{-1}$, $\lambda_P = 0.02V^{-1}$

and Table 3.1-2 values;

$$A_V = \frac{2\sqrt{(17)(8)(5)(5)}}{(0.015+0.02)^2\sqrt{I_1 I_6}} \cdot 10^{-6} = \frac{95199 \cdot 10^{-6}}{\sqrt{I_1 I_6}}$$

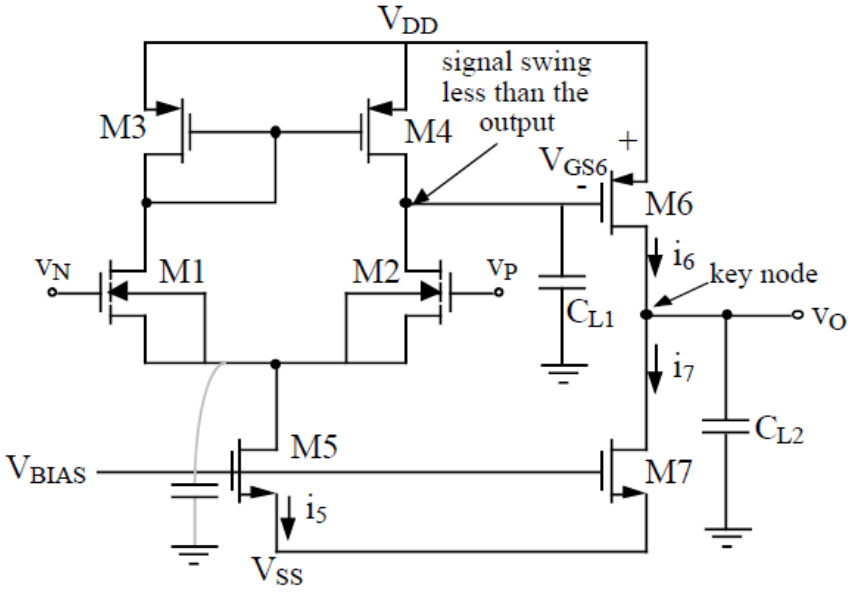
Assume $I_1 = 10\ \mu A$ and $I_6 = 100\ \mu A$

$$\underline{\underline{A_V = 3010}}$$

$$\frac{V_{OH} - V_{OL}}{A_V} = \text{Resolution} = 5\ \text{mV (assume)}$$

then $V_{OH} - V_{OL} = \frac{5}{1000} \cdot 3000 = 15\ \text{Volts}$

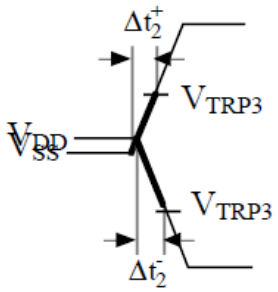
PROPAGATION DELAY OF THE TWO-STAGE COMPARATOR



$$V_{GS6} = V_{DD} - (v_P + V_{DG2})$$

$i_C = C\frac{dv}{dt}$, $\Delta t = C\frac{\Delta v}{I}$

$$\Delta t_2+ = C_{L2}\left[\frac{V_{TRP3} - V_{SS}}{\frac{K_P W_6}{2\ L_6}(V_{DD} - v_P - V_{DG2} - |V_{T6}|)^2 - I_7}\right]$$

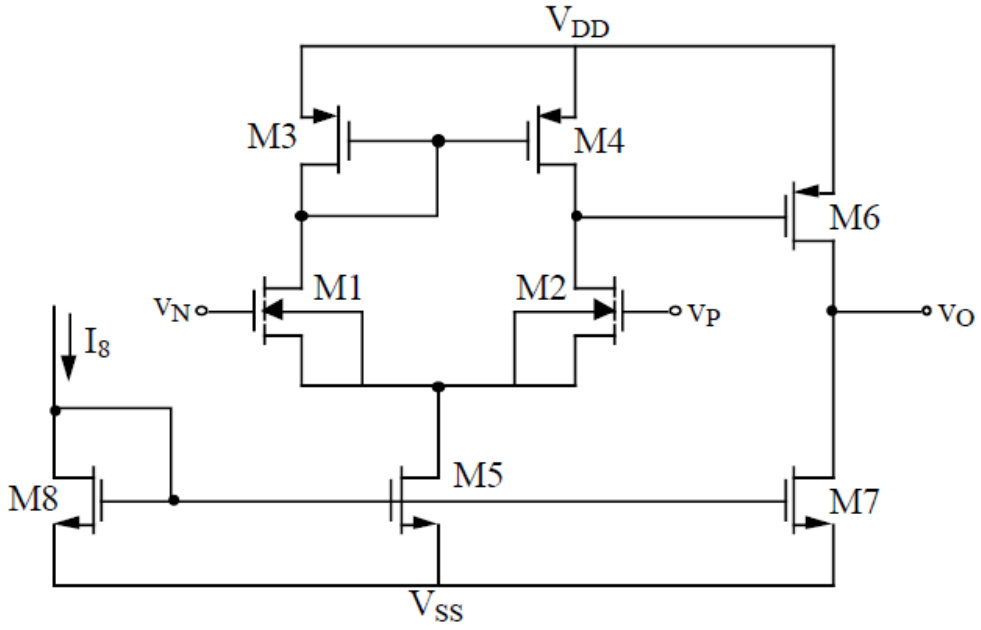


$$\Delta t_2- = C_{L2}\left[\frac{V_{DD} - V_{TRP3}}{\left(\frac{W_7}{L_7}\right)\left(\frac{L_5}{W_5}\right) i_5}\right]$$

$$\text{Slew rate} = \frac{i_{source/sink}}{C_{Li}}$$

TWO-STAGE, CMOS COMPARATOR

General Schematic



Key Relationships for Design:

$$\boxed{i_D = \frac{\beta}{2}(v_{GS} - V_T)^2} \quad \Rightarrow \quad i_D(sat) = \frac{\beta}{2}[v_{DS}(sat)]^2$$

or

$$\boxed{v_{DS}(sat) = \sqrt{\frac{2i_D(sat)}{\beta}}}$$

Also,

$$\boxed{g_m = \sqrt{2\beta I_D}}$$

where

$$\beta = \frac{KW}{L}$$

COMPARATOR DESIGN PROCEDURE

1. Set the output current to meet the slew rate requirements.

$$i = C\frac{dV}{dt}$$

2. Determine the minimum sizes for M6 and M7 for the proper ouput voltage swing.

$$v_{DS}(sat) = \sqrt{\frac{2I_D}{\beta}}$$

3. Knowing the second stage current and minimum device size for M6, calculate the second stage gain.

$$A_2 = \frac{-g_{m6}}{g_{ds6} + g_{ds7}}$$

4. Calculate the required first stage gain from A_2 and gain specifications.
5. Determine the current in the first stage based upon proper mirroring and minimum values for M6 and M7. Verify that P_{diss} is met.
6. Calculate the device size of M1 from A_1 and I_{DS1}.

$$A_1 = \frac{-g_{m1}}{g_{ds1} + g_{ds3}} \quad \text{and} \quad g_{m1} = \sqrt{\frac{2K'W/L}{I_{DS1}}}$$

7. Design minimum device size for M5 based on negative CMR requirement using the following ($I_{DS1} = 0.5I_{DS5}$):

$$v_{G1}(min) = V_{SS} + V_{DS5} + \sqrt{\frac{I_{DS5}}{\beta_1}} + V_{T1}(max)$$

$$\text{where } V_{DS5} = \sqrt{\frac{2I_{DS5}}{\beta_5}} = V_{DS5}(sat)$$

8. Increase either M5 or M7 for proper mirroring.
9. Design M4 for proper positive CMR using:

$$v_{G1}(max) = V_{DD} - \sqrt{\frac{I_{DS5}}{\beta_3}} - \left|V_{TO3}\right|(max) + V_{T1}$$

10. Increase M3 or M6 for proper mirroring.
11. Simulate circuit.

DESIGN OF A TWO-STAGE COMPARATOR

Specifications:

$A_{vo} > 66$ dB Lambda = $0.05V^{-1}$ (L = 5 µm)

$P_{diss} < 10$ mW $V_{DD} = 10$ V

$C_L = 2$ pF $V_{SS} = 0$ V

$t_{prop} < 1$ µs Recall that $\beta = \frac{K'W}{L}$

CMR = 4-6 V

Output swing is V_{DD} - 2V and V_{SS} + 2V

1). For $t_{prop} << 1$ µs choose slew rate at 100 V/µs

$$\therefore\ I_7 = C_L\frac{dv_{OUT}}{dt} = (2\cdot10^{-12})(100\cdot10^{-6}) = 200\ \mu A$$

2). Size M6 and M7 to get proper output swing,

M7:

$$2V > v_{DS7}(sat) = \sqrt{\frac{2I_7}{\beta_7}} = \sqrt{\frac{2(200\mu A)}{17.0\mu A/V^2(W_7/L_7)}} \rightarrow \underline{\underline{\frac{W_7}{L_7} > 5.88}}$$

M6:

$$2V > v_{DS6}(sat) = \sqrt{\frac{2(I_{OUT}+I_7)}{\beta_6}} = \sqrt{\frac{2(400\mu A)}{8.0\mu A/V^2(W_6/L_6)}} \rightarrow \underline{\underline{\frac{W_6}{L_6} > 12.5}}$$

3). $$A_2 = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \left(\frac{-1}{\lambda_N + \lambda_P}\right)\sqrt{\frac{2K_P'W_6}{I_6L_6}} \approx -10$$

4). $A_{vo} = A_1A_2 = 66$ dB $\approx 2000 \rightarrow A_1 = 200$

5). Assuming $v_{GS4} = v_{GS6}$, then $I_4 = \frac{S_4}{S_6} I_6$

choose $S_4 = 1$ which gives $I_4 = \frac{1}{12.5}(200\mu A) = 16.0\ \mu A$

Assume $S_5 = 1$ which gives $I_5 = \frac{S_5}{S_7} I_7 = \frac{200\mu A}{5.88} = 34\ \mu A$

and $I_4 = \frac{1}{2} I_5 = 17\ \mu A$

Choose $\underline{\underline{I_4 = 17\ \mu A}}$ to keep $\frac{W}{L}$ ratios greater than 1.

$\therefore I_5 = 34\ \mu A \qquad \frac{W_4}{L_4} = \frac{W_6}{L_6}\left(\frac{17}{200}\right) = 1.06 \approx 1.0$

$P_{diss} = 10(I_7 + I_5) = 2.34\ mW < 10\ mW$

6). $A_1 = \frac{1}{\lambda_1 + \lambda_4}\sqrt{\frac{2K_N'W_1}{I_4L_1}} \rightarrow \frac{W_1}{L_1} = [(\lambda_1 + \lambda_4)A_1]^2 \frac{I_4}{2K_N'} = 200$

$\therefore \underline{\underline{\frac{W_1}{L_1} = 200}}$ (Good for noise)

7). $V_{DS5} = v_{G1}(min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(max)$

$V_{DS5} = 4 - 0 - \sqrt{\frac{(34)}{2(17.0)(200)}} - 1 = 2.90\ V$

$V_{DS5} = \sqrt{\frac{2I_5}{\beta_5}} = \sqrt{\frac{2(34\mu)}{(17\mu)S_5}} \rightarrow \frac{W_5}{L_5} > 0.48$

8). $S_5 = \frac{I_5}{I_7} S_7 = \frac{34}{200}(5.88) = 1.0 \rightarrow \underline{\underline{\frac{W_5}{L_5} = 1.0}}$

9). $V_{G1}(max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{TO3}|(max) + V_{T1}(min)$

$$\beta_3 = \frac{I_5}{\left[V_{DD} - V_{G1}(max) - |V_{TO3}|(max) + V_{T1}(min)\right]^2}$$

$$= \frac{34\ \mu A}{(10 - 6 - 1 + 0.5)^2} = 2.76 \cdot 10^{-6}$$

$$\therefore \frac{W_3}{L_3} = \frac{(2.76)(2)}{8} = 0.69 \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} > 0.69$$

(Previously showed $\frac{W_4}{L_4} > 1.06$ so no modification is necessary)

10). Summary

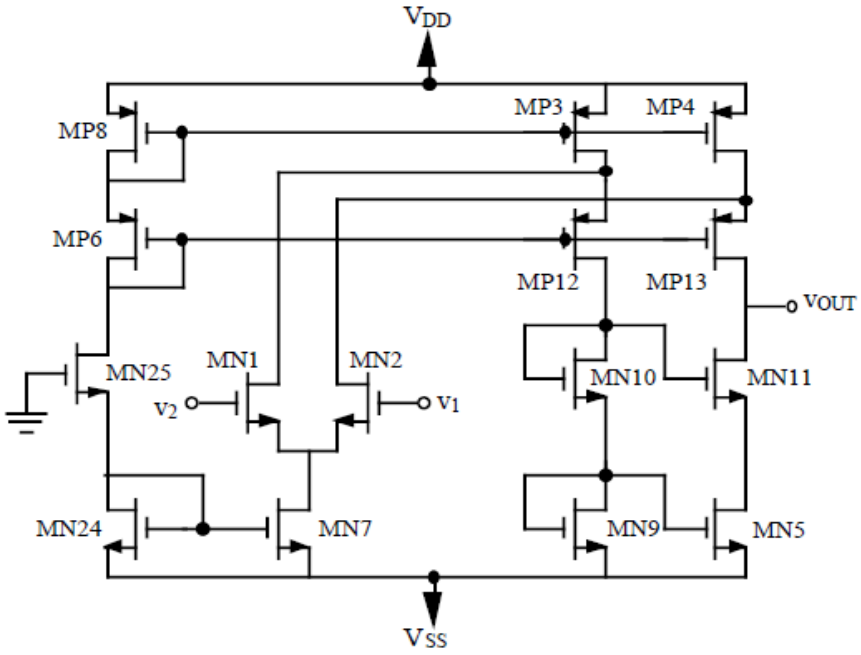
$$W_{drawn} = \left(\frac{W}{L}\right)(L - 1.6)$$

Design Ratios	Actual Values with 5μm minimum geometry	Proper Mirroring and $L_D = 0.8\mu m$
$\frac{W_1}{L_1} = \frac{W_2}{L_2} = 200$	$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{1000}{5}$	$\frac{680}{5}$
$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 1.0$	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{5}{5}$	$\frac{3.4}{5}$, $\frac{5}{5}$
$\frac{W_5}{L_5} = 1.0$	$\frac{W_5}{L_5} = 1.0$	$\frac{3.4}{5}$, $\frac{5}{5}$
$\frac{W_6}{L_6} = 12.5$	$\frac{W_6}{L_6} = \frac{62.5}{5}$	$\frac{60}{5}$
$\frac{W_7}{L_7} = 5.88$	$\frac{W_7}{L_7} = \frac{30}{5}$	$\frac{30}{5}$

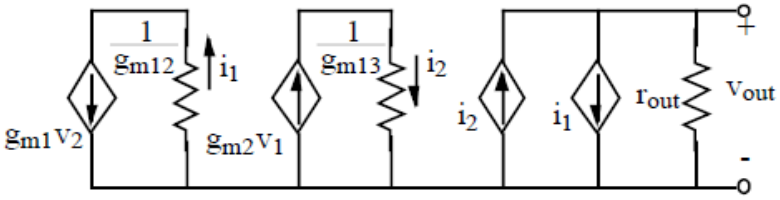
(Need to adjust for proper mirroring) $\Rightarrow$ $\frac{S_6}{S_4} = 2\frac{S_7}{S_5}$

FOLDED CASCODE CMOS COMPARATOR

Circuit Diagram



Small Signal Model



where

$$R_{out} \approx (r_{ds5}g_{m11}r_{ds11})||((r_{ds4}||r_{ds2})g_{m13}r_{ds13}) =$$

$$= \frac{1}{\frac{g_{ds5}g_{ds11}}{g_{m11}} + \frac{(g_{ds2}+g_{ds4})g_{ds13}}{g_{m13}}}$$

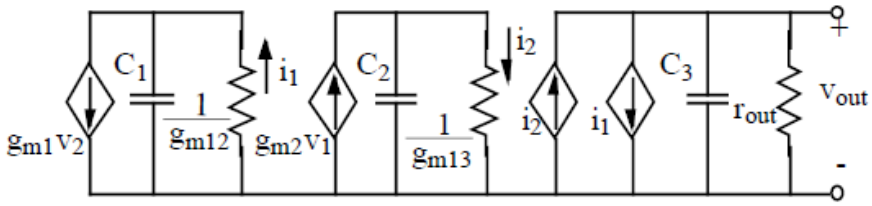
The small signal voltage gain is

$$v_{out} = r_{out}(i_2-i_1) = (g_{m2}+g_{m1})R_{out}v_{in} = \left(\frac{g_{m1}+g_{m2}}{\frac{g_{ds5}g_{ds11}}{g_{m11}} + \frac{(g_{ds2}+g_{ds4})g_{ds13}}{g_{m13}}} \right) v_{in}$$

where $v_{in} = v_1 - v_2$.

Frequency Response

Small signal model-



where

$$C_1 = C_{GS12} + C_{BS12} + C_{DG3} + C_{BD3}$$

$$C_2 = C_{GS13} + C_{BS13} + C_{DG4} + C_{BD4}$$

and $$C_3 = C_{DG11} + C_{BD11} + C_{DG13} + C_{BD13} + C_{Load}$$

$$A_{VD}(s) \approx \frac{A_{VD0}\omega_3}{s + \omega_3}$$

where

$$\omega_3 = \frac{1}{r_{out}C_3}$$

Typical performance-

$I_{D1} = I_{D2} = 50\mu A$ and $I_{D3} = I_{D4} = 100\mu A$, $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_{11}}{L_{11}} = \frac{W_{13}}{L_{13}}$ =1, assume $C_3 \approx 0.5pF$, and using the values of Table 3.1-2 gives:

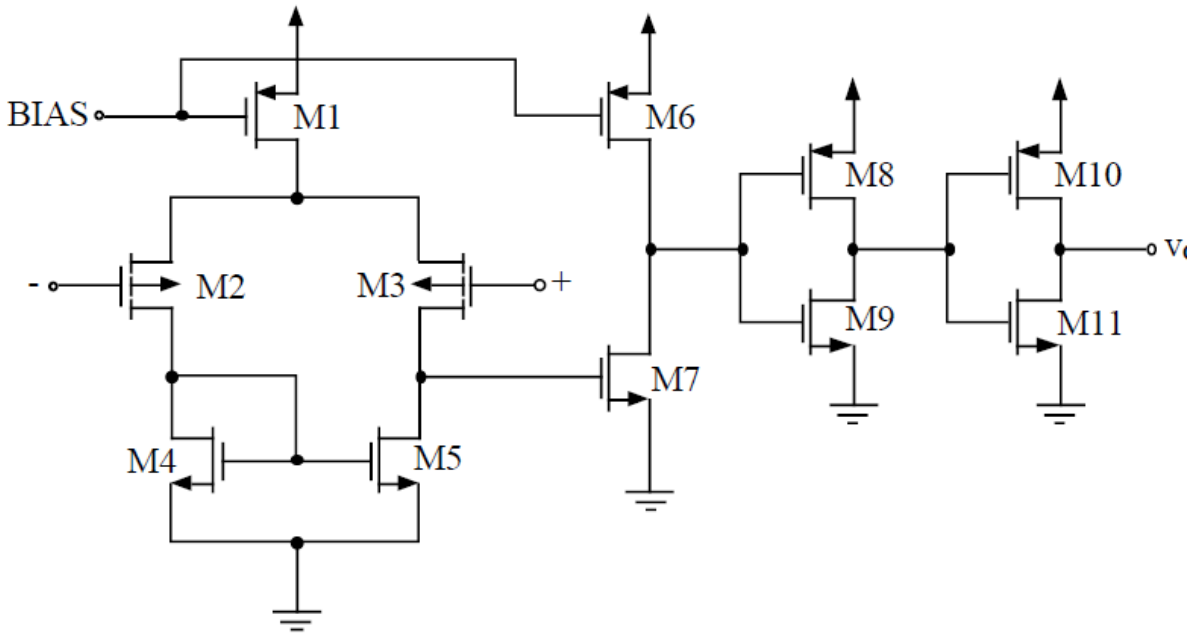
$$g_{m1} = g_{m2} = g_{m11} = 41.2\mu S \qquad g_{m13} = 28.3\mu S$$

$$g_{ds5} = g_{ds11} = 0.5\mu S \qquad g_{ds4} = g_{ds13} = 0.25\mu S$$

Therefore, $r_{out} = 121M\Omega$, $\omega_3 = 16.553krps$, and $A_{VD0} = 4{,}978$ resulting in a gain-bandwidth of 13.11MHz.

$$\text{Delay} = \Delta T = \frac{C_3\Delta V}{I_{max}} = \frac{0.5pF \times 10V}{100\mu A} = 50nS$$

OPEN LOOP COMPARATOR - MC 14575



Performance (I_{SET} = 50 µA)

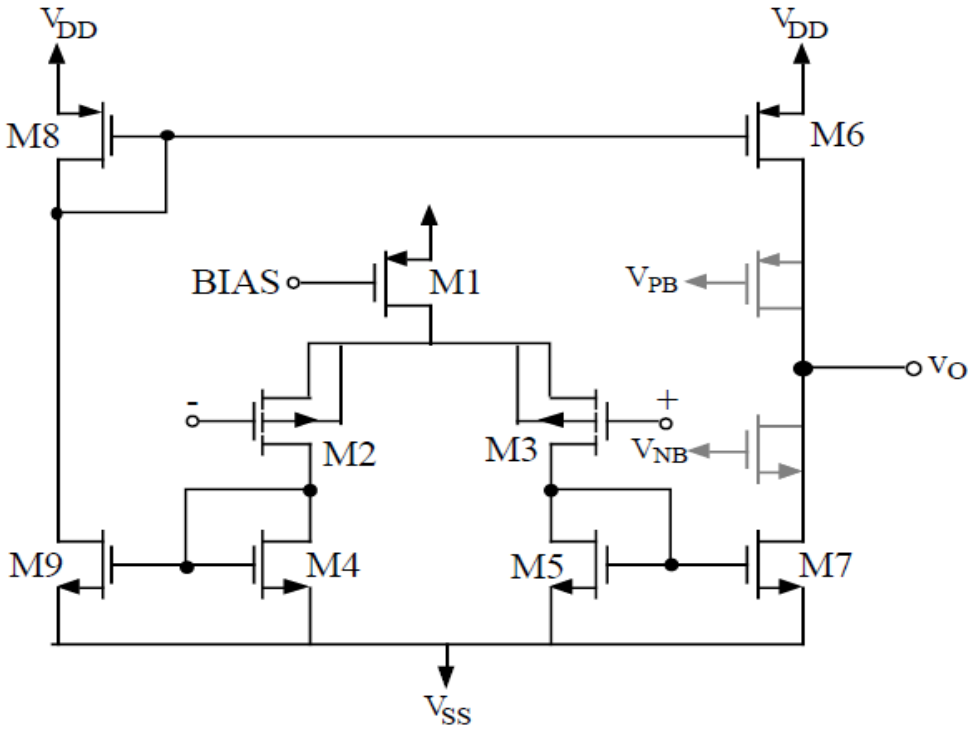
$$\frac{\text{Rise time}}{\text{Fall time}} = 100 \text{ ns into } 50 \text{ pF}$$

Propagation delay = 1 µs

Slew rate = 2.7 Volts/µs

Loop Gain = 32,000

CLAMPED CMOS VOLTAGE COMPARATOR



Drain of M2 and M3 clamped to the gate voltages of M4 and M5.

M6 and M7 provide a current, push-pull output drive capability similiar to the current , push-pull CMOS OP amp.

Comparator is really a voltage comparator with a current output.

Improving the Performance of Open-Loop Comparators:

There are two areas in which the performance of an open-loop, high-gain comparator can be improved with little extra effort. These areas are the input-offset voltage and a single transition of the comparator in a noisy environment. The first problem can be solved by *autozeroing* and the second can be solved by the introduction of hysteresis using a bistable circuit. These two techniques will be examined in the following.

Autozeroing Techniques

Input-offset voltage can be a particularly difficult problem in comparator design. In precision applications, such as high-resolution A/D converters, large input-offset voltages cannot be tolerated. While systematic offset can nearly be eliminated with proper design (though still affected by process variations), random offsets still remain and are unpredictable. Fortunately, there are techniques in MOS technology to remove a large portion of the input offset using offset-cancellation techniques. These techniques are available in MOS because of the nearly infinite input resistance of MOS transistors. This characteristic allows long-term storage of voltages on the transistor's gate. As a result, offset voltages can be measured, stored on capacitors, and summed with the input so as to cancel the offset.

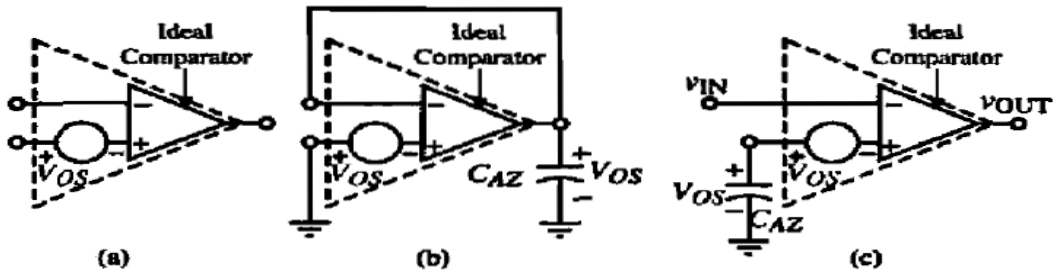


Figure 8.4-1 (a) Simple model of a comparator including offset. (b) Comparator in unity-gain configuration storing the offset on autozero capacitor C_{AZ} during the first half of the autozero cycle. (c) Comparator in open-loop configuration with offset cancellation achieved at the noninverting input during the second half of the autozero cycle.

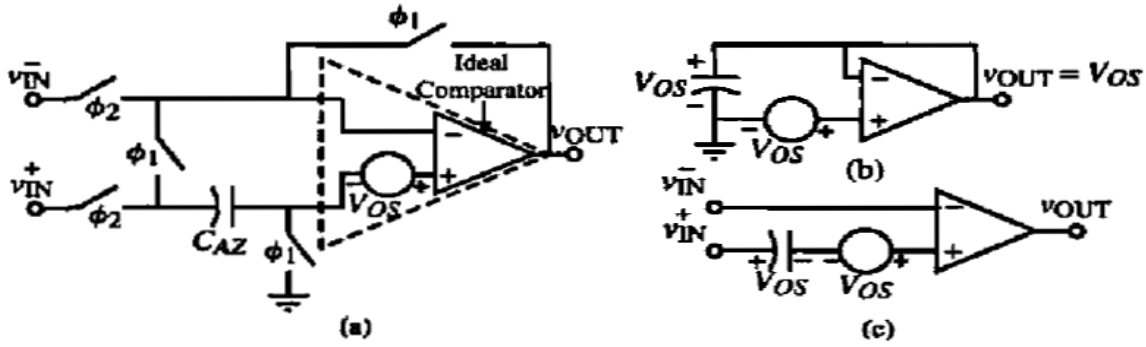


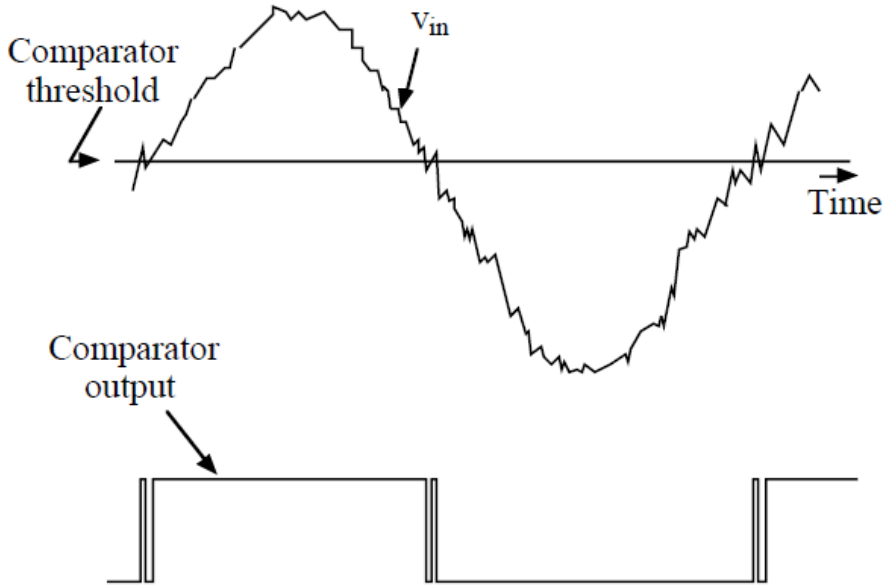
Figure 8.4-2 (a) Differential circuit implementation of an autozeroed comparator. (b) Comparator during ϕ_1 phase. (c) Comparator during ϕ_2 phase.

Comparator with hysteresis:

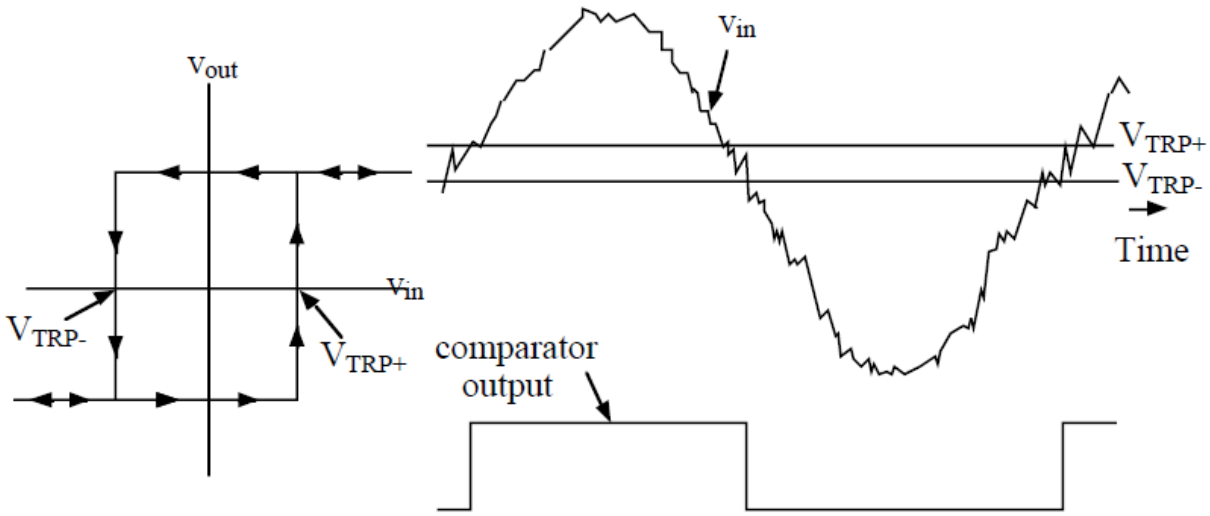
Why Hysteresis?

Eliminates "chattering" when the input is noisy.

Comparator with no Hysteresis

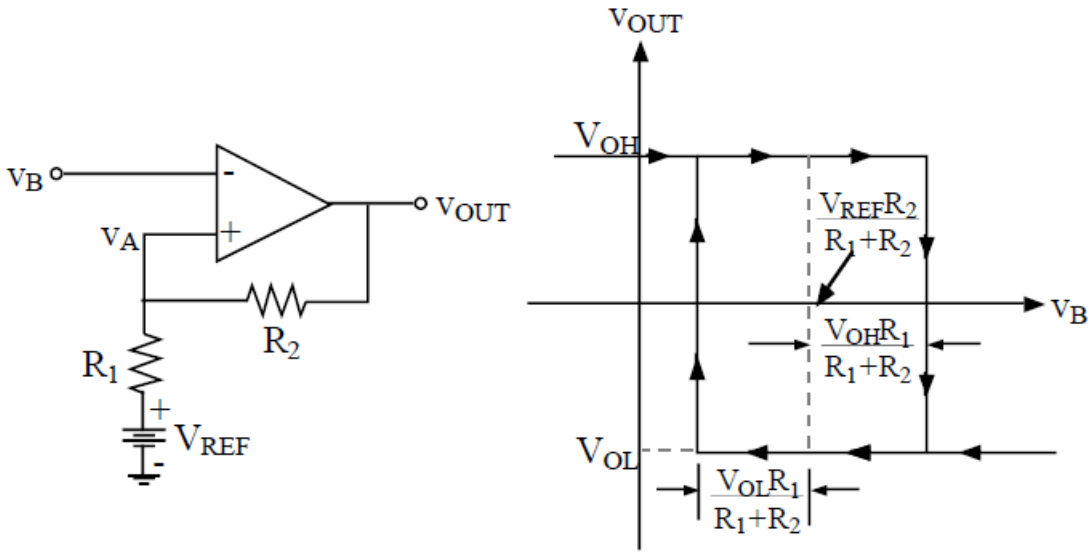


Comparator with Hysteresis

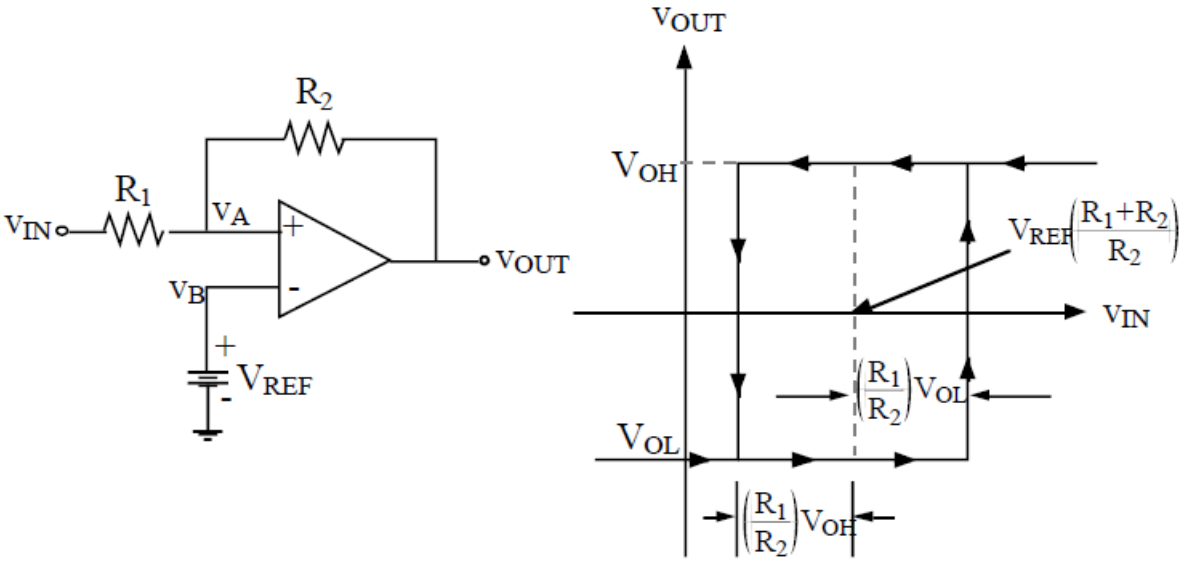


VOLTAGE COMPARATORS USING EXTERNAL FEEDBACK

Inverting



Noninverting



DESIGN OF AN INVERTING COMPARATOR WITH HYSTERESI

Use the circuit of Fig. 8.4-10 to design a high-gain, open-loop comparator having an uppe trip point of 1 V and a lower trip point of 0 V if $V_{OH} = 2$ V and $V_{OL} = -2$ V.

Solution

Putting the values of this example into Eqs. (8.4-13) and (8.4-14) gives

$$1 = \left(\frac{R_1}{R_1 + R_2}\right)2 + \left(\frac{R_1}{R_1 + R_2}\right)V_{REF}$$

and

$$0 = \left(\frac{R_1}{R_1 + R_2}\right)(-2) + \left(\frac{R_1}{R_1 + R_2}\right)V_{REF}$$

Solving these two equations gives $3R_1 = R_2$ and $V_{REP} = 2$ V.

Discrete-Time Comparators:

In many applications the comparator only functions over a portion of a time period. Such circuits are driven by a clock and will have a portion of time or phase when the comparator is functioning as a comparator and a phase when the comparator is not being used. In this circumstance, other forms of comparators can be used that are efficient and have a small propagation delay time. We will examine two such comparators in this section. They are the switched capacitor comparator and the regenerative comparator.

Switched Capacitor Comparators

The switched capacitor comparator uses a combination of switched capacitors and open-loop comparators. The advantages of the switched capacitor comparator are that differential signals can be compared using single-ended circuits and the switched capacitor comparator naturally lends itself to autozeroing the dc offset voltage of the open-loop comparator. Figure 8.5-1(a) shows a typical switched capacitor comparator. The voltages applied to the circuit are normally sampled and held so that capital variables are used.

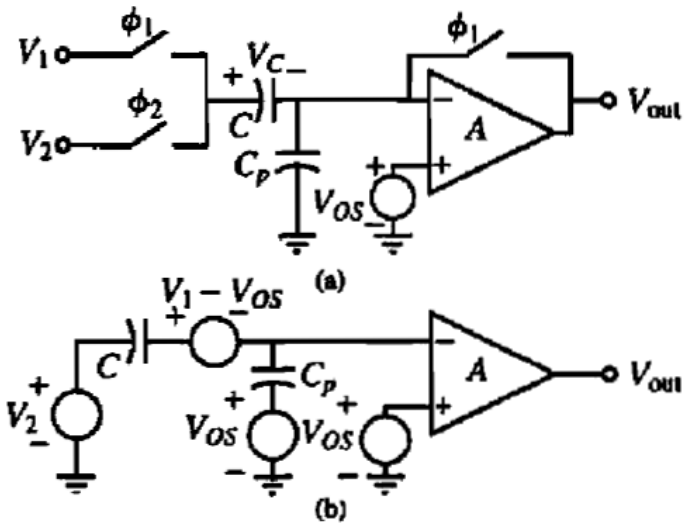


Figure 8.5-1 (a) A switched capacitor comparator. (b) Equivalent circuit of (a) when the ϕ_2 switches are closed.

$$V_C(\phi_1) = V_1 - V_{OS}$$

and

$$V_{C_p}(\phi_1) = V_{OS}$$

$$V_{out}(\phi_2) = -A\left[\frac{V_2 C}{C + C_p} - \frac{(V_1 - V_{OS})C}{C + C_p} + \frac{V_{OS}C_p}{C + C_p}\right] + AV_{OS}$$

$$= -A\left[(V_2 - V_1)\frac{C}{C + C_p} - V_{OS}\left(\frac{C}{C + C_p} + \frac{C_p}{C + C_p}\right)\right] + AV_{OS} = -A(V_2 - V_1)\frac{C}{C + C_p}$$

$$V_{out}(\phi_2) \approx A(V_1 - V_2)$$

Therefore, the difference between the voltages V_1 and V_2 is amplified by the gain of the comparator.

Regenerative Comparators

Regenerative comparators use positive feedback to accomplish the comparison of two signals. The regenerative comparator is also called a *latch* or a *bistable* [5]. The simplest form of a latch is shown in Fig. 8.5-3 and consists of two cross-coupled MOSFETs. Figure 8.5-3(a) uses NMOS transistors while Fig. 8.5-3(b) is a PMOS latch. The current sources/sinks are used to identify the dc currents in the transistors. Normally, the latch has two modes of operation. The first mode disables the positive feedback and applies the input signal to the terminals designated as v_{o1} and v_{o2}. The initial voltages applied during this mode will be designated as v'_{o1} and v'_{o2}. The second mode enables the latch and depending on the relative values of v'_{o1} and v'_{o2}, one of the outputs will go high and the other will go low. A two-phase clock is used to determine the modes of operation.

It is important to characterize the time it takes for the latch to go from its initial state the final state during the enabled mode of operation. Figure 8.5-4(a) is a redrawing of

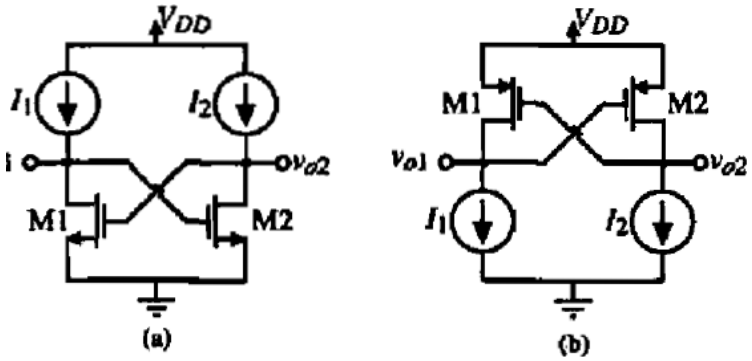


Figure 8.5-3 (a) NMOS latch. (b) PMOS latch.

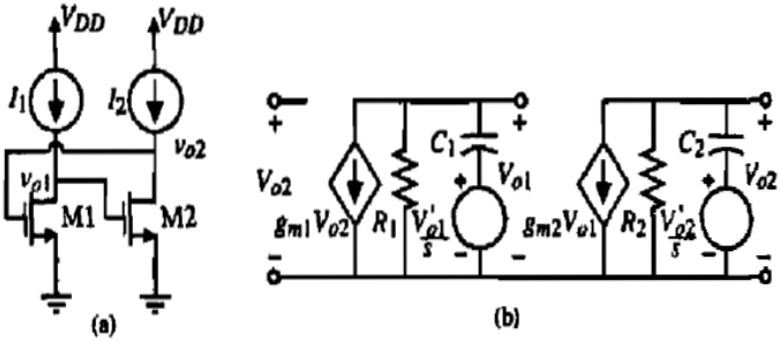


Figure 8.5-4 (a) Redrawing of Fig. 8.5-3(a). (b) Equivalent model of (a).

$$g_{m1}V_{o2} + G_1V_{o1} + sC_1\left(V_{o1} - \frac{V_{o1}}{s}\right) = g_{m1}V_{o2} + G_1V_{o1} + sC_1V_{o1} - C_1V'_{o1} = 0$$

and

$$g_{m2}V_{o1} + G_2V_{o2} + sC_2\left(V_{o2} - \frac{V'_{o2}}{s}\right) = g_{m2}V_{o1} + G_2V_{o2} + sC_2V_{o2} - C_2V'_{o2} = 0$$

where G_1 and G_2 are the conductances seen from the drains of M1 and M2 to ground and C_1 and C_2 are the capacitances seen from the drains of M1 and M2 to ground. Solving Eqs. (8.5-5) and (8.5-6) for V_{o1} and V_{o2} gives

$$V_{o1} = \frac{R_1C_1}{sR_1C_1 + 1}V'_{o1} - \frac{g_{m1}R_1}{sR_1C_1 + 1}V_{o2} = \frac{\tau_1}{s\tau_1 + 1}V'_{o1} - \frac{g_{m1}R_1}{s\tau_1 + 1}V_{o2}$$

$$V_{o2} = \frac{R_2C_2}{sR_2C_2 + 1}V'_{o2} - \frac{g_{m2}R_2}{sR_2C_2 + 1}V_{o1} = \frac{\tau_2}{s\tau_2 + 1}V'_{o2} - \frac{g_{m2}R_2}{s\tau_2 + 1}V_{o1}$$

where τ_1 is the time constant R_1C_1. Assume that both transistors are identical so that $g_{m1} = g_{m2} = g_m$, $R_1 = R_2 = R$, and $C = C_1 = C_2$, which gives $\tau_1 = \tau_2 = \tau$. Let us define the difference between V_{o2} and V_{o1} as ΔV_o and the difference between V'_{o2} and V'_{o1} as ΔV_i. Therefore,

$$\Delta V_o = V_{o2} - V_{o1} = \frac{\tau}{s\tau + 1}\Delta V_i + \frac{g_mR}{s\tau + 1}\Delta V_o$$

Solving for ΔV_o gives

$$\Delta V_o = \frac{\tau\,\Delta V_i}{s\tau + (1 - g_mR)} = \frac{\dfrac{\tau\,\Delta V_i}{1 - g_mR}}{\dfrac{s\tau}{1 - g_mR} + 1} = \frac{\tau'\,\Delta V_i}{s\tau' + 1}$$

where

$$\tau' = \frac{\tau}{1 - g_mR}$$

Tutorial Problems

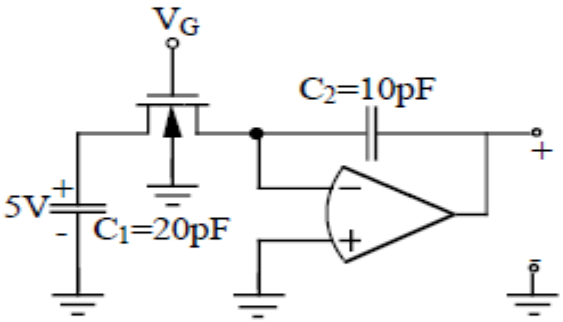
1. What is the on resistance of an enhancement MOS switch if $V_S = 0V$, V_G = 10V, W/L = 1, $V_{TO} = 1V$, and $K' = 25\mu A/V^2$?

Assume that $v_{DS} \approx 0V$. Therefore,

$$R_{ON} \approx \frac{v_{DS}}{i_D} = \frac{L/W}{K'(V_G - V_S - V_T)}$$

$$R_{ON} = \frac{10^6}{25(10-1)} = 4444\Omega$$

2. If V_G=10V at t=0, what is the W/L value necessary to discharge C_1 to with 5% of its intial charge at t=0.1μS? Assume $K'=25\mu A/V^2$ and $V_{TO} = 1V$.



$$v(t) = 5\exp(-t/RC) \rightarrow \exp\left(\frac{10^{-7}}{RC}\right) = 20 \rightarrow RC = \frac{10^{-7}}{\ln(20)}$$

$$\text{Therefore, } R = \frac{10}{6} \text{ x } 10^3\Omega$$

$$\text{Thus, } \frac{10x10^3}{6} = \frac{L/W}{K'(V_G - V_S - V_T)} = \frac{L/W}{(2.5x10^{-5})(9)}$$

$$\text{Gives } \frac{W}{L} = 2.67$$

3. Assume that V_{DD} varies from 8 to 12 volts and that V_{SS} = 0. Using the values of Table 3.1-2, find the common mode range for worst case conditions. Assume that I_{SS} = 100μA, $W_1/L_1 = W_2/L_2$ = 5, $W_3/L_3 = W_4/L_4$ = 1, and v_{SD5} = 0.2V. Include the worst case value of K' in the calculations.

If V_{DD} varies 10 ± 2V, then we get

$$v_{G1(max)} = V_{DD} - v_{SD5} - \sqrt{\frac{I_{SS}}{\beta_1}} - |V_{T1}|$$

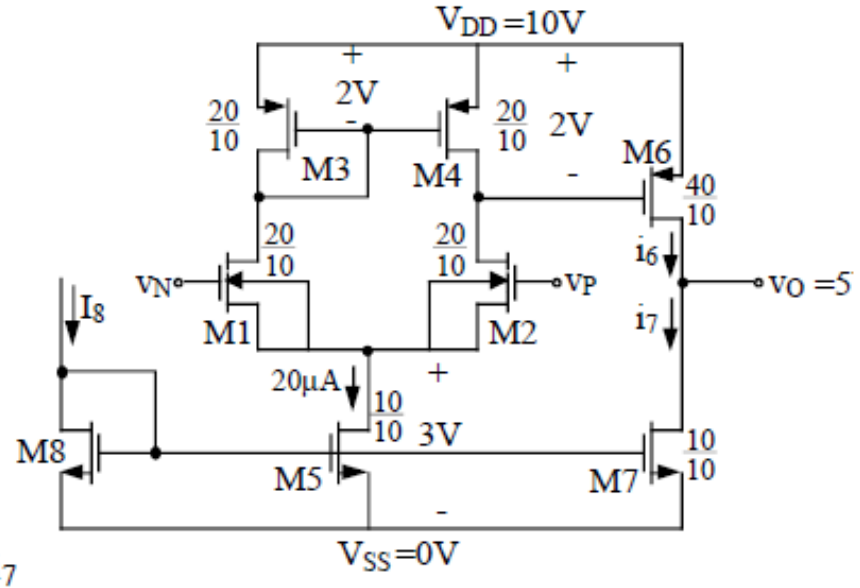
$$= 8 - 0.2 - \sqrt{\frac{100}{5x7.2}} - 1.2 = 6.6 - 1.67 = 4.99V$$

$$v_{G1(min)} = V_{SS} + \sqrt{\frac{I_{SS}}{\beta_3}} + V_{TO3} - |V_{T1}|$$

$$= 0 + \sqrt{\frac{100}{1x18.7}} + 1.2 - 0.8 = 0.4 + 2.31 = 2.71V$$

4. Therefore, the input common mode range of the p-channel input differential amplifier is from 2.71V to 4.99V

$K_N = 24.75\ \mu A/V^2$
$K_P = 10.125\ \mu A/V^2$
$V_{TN} = -V_{TP} = 1V$
$\lambda_N = 0.015V^{-1}$
$\lambda_P = 0.020V^{-1}$



Find V_{OS} to make $i_6 = i_7$

(1) Find the mismatch between i_6 and i_7

$$\frac{i_7}{i_5} = \left(\frac{1 + \lambda_N v_{DS7}}{1 + \lambda_N v_{DS5}}\right)\left(\frac{W_7/L_7}{W_5/L_5}\right) = \frac{1 + (0.015)(5)}{1 + (0.015)(3)}(1) = 1.029$$

$$\frac{i_6}{i_4} = \left(\frac{1 + \lambda_P v_{DS6}}{1 + \lambda_P v_{DS4}}\right)\left(\frac{W_6/L_6}{W_4/L_4}\right) = \frac{1 + (0.02)(5)}{1 + (0.02)(2)}(2) = 2.115$$

$i_5 = 2i_4$

$\therefore\ i_7 = (1.029)(2)i_4 = 2.057i_4$ and $i_6 = 2.115i_4$

(2) Find how much v_{GS6} must be reduced to make $i_6 = i_7$

$\Delta v_{GS6} = v_{GS6}(2.115i_4) - v_{GS6}(2.057i_4)$

$$\Delta v_{GS6} = \sqrt{\frac{2L_6}{K_P W_6}\, i_4}\left(\sqrt{2.115} - \sqrt{2.057}\right) = 14.11\ \text{mV}$$

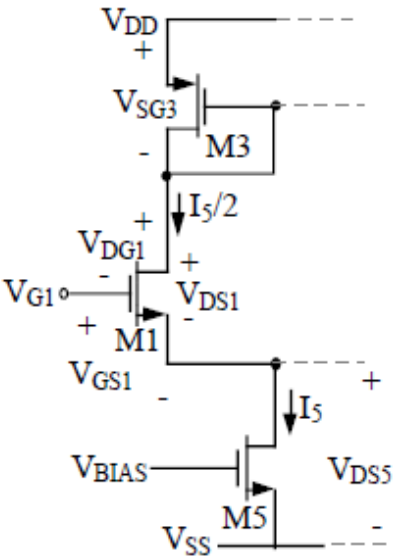
(3) Reflecting Δv_{GS6} into the input

$$A_v(\text{diff}) = \left(\frac{2}{\lambda_2 + \lambda_4}\right)\sqrt{\frac{K_N(W_2/L_2)}{I_5}} = 89.9$$

$$\therefore\ V_{OS} = \frac{\Delta v_{GS6}}{A_v(\text{diff})} = \frac{14.1\ \text{mV}}{89.9} = \underline{0.157\ \text{mV}}$$

5.

DESIGNING FOR COMMON MODE INPUT RANGE



$$v_{G1}(\min) = V_{SS} + V_{DS5} + V_{GS1}$$

$$\boxed{v_{G1}(\min) = V_{SS} + V_{DS5} + V_{T1}(\max) + \sqrt{\frac{I_5}{2\beta_1}}}$$

$$v_{G1}(\max) = V_{DD} - V_{SG3} - V_{DG1}(\text{sat})$$

$$\boxed{v_{G1}(\max) = V_{DD} - \sqrt{\frac{I_5}{2\beta_3}} - \left|V_{T3}(\max)\right| + V_{T1}(\min)}$$

where $V_{DG1}(\text{sat}) = -V_{T1}$

Example

Design M1 through M4 for a CM input range 1.5 to 9 Volts when V_{DD} = 10 V, I_{SS} = 40μA, and V_{SS} = 0V. Table 3.1-2 parameters with $|V_{TN,P}|$ = 0.4 to 1.0 Volts,

$$v_{G1}(\min) = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max)$$

$$1.5 = 0 + 0.1 + \sqrt{\frac{40\mu A}{\beta_1}} + 1 \quad \text{(assumed } V_{DS5} \approx 0.1\text{V- it probably more reasonable to assume } \beta_1 \text{ is already defined and find } \beta_5\text{)}$$

$$\beta_1 = \frac{K_N W_1}{L_1} = 250\ \mu A/V^2 \cdot \quad \boxed{\frac{W_1}{L_1} = \frac{W_2}{L_2} = 14.70}$$

$$v_{G1}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T3}(\max)| + V_{T1}(\min)$$

$$\beta_3 = \frac{K_P W_3}{L_3} = 250\ \mu A/V^2 \cdot \quad \boxed{\frac{W_3}{L_3} = \frac{W_4}{L_4} = 31.25}$$

Example: Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1μm.

$A_v > 3000$V/V	$V_{DD} = 2.5$V	$V_{SS} = -2.5$V
$GB = 5$MHz	$C_L = 10$pF	$SR > 10$V/μs
V_{out} range $= \pm 2$V	$ICMR = -1$ to 2V	$P_{diss} \leq 2$mW

Solution

Calculate the minimum value of the compensation capacitor C_c.

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3 \times 10^{-12})(10 \times 10^6) = 30\ \mu\text{A}$$

Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(50 \times 10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 15$$

$$g_{m3} = \sqrt{2 \times 50\text{x}10^{-6}\ \text{x}15\text{x}10^{-6} \times 15} = 150\mu\text{S}$$

Therefore

$$(W/L)_3 = (W/\text{L})_4 = 15$$

Check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 0.4\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = 15.75\text{x}10^9(\text{rads/sec})$$

or 2.98 GHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

The next step in the design is to calculate g_{m1}

$$g_{m1} = (5 \times 10^6)(2\pi)(3 \times 10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{{g_{m1}}^2}{2K'_N I_1} = \frac{(94.25)^2}{2 \cdot 110 \cdot 15} = 2.79 \approx 3.0$$

Next calculate V_{DS5}

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30 \times 10^{-6}}{110 \times 10^{-6} \cdot 3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from Eq. (16)

$$(W/L)_5 = \frac{2(30 \times 10^{-6})}{(50 \times 10^{-6})(0.35)^2} = 4.49 \approx 4.5$$

From Eq. (20) of Sec. 6.2, we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$

$$(W/L)_6 = 15 \frac{942.5 \times 10^{-6}}{150 \times 10^{-6}} = 94.25$$

Using the equations for proper mirroring, I_6 is determined to be

$$I_6 = (15 \times 10^{-6})(94.25/15) = 94.25\ \mu\text{A}$$

Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5 \left(\frac{94.25 \times 10^{-6}}{30 \times 10^{-6}} \right) \approx 14.14$$

Check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{min}(\text{out}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \times 94.25}{110 \times 14.14}} = 0.348\text{V}$$

which is much less than required. At this point, the first-cut design is complete.

7. Examining the results shows that the large value of M7 is due to the large value of M5 which in turn is due to a tight specification on the negative input common a

Calculate the gain, unity-gain bandwidth, and slew rate of the previous two-stage op amp used in weak inversion if:

$I_{D5} = 200\text{nA}$	$n_P = 1.5$	$\lambda_P = 0.02\text{V}^{-1}$
$L = 10\ \mu\text{m}$	$n_N = 2.5$	$\lambda_N = 0.01\text{V}^{-1}$
$C = 5\text{pF}$	$T = 27^\circ\text{C}$	

$$A_V = \frac{1}{(1.5)(2.5)(0.026)(2)(0.1+0.02)(0.01+0.02)} = 5698$$

8

$$GB = \frac{100 \cdot 10^{-9}}{(2.5)(0.026)(5 \cdot 10^{-12})} = 307.69\text{Krps or } 48.97\text{KHz}$$

Find the propagation delay time of an open loop comparator that has a dominant pole at 10^3 radians/sec, a dc gain of 10^4, a slew rate of $1\text{V}/\mu\text{s}$, and a binary output voltage swing of 1V. Assume the applied input voltage is 10mV.

Solution

The input resolution for this comparator is $1\text{V}/10^4$ or 0.1mV. Therefore, the 10mV input is 100 times larger than v_{in}(min) giving a k of 100. Therefore, we get

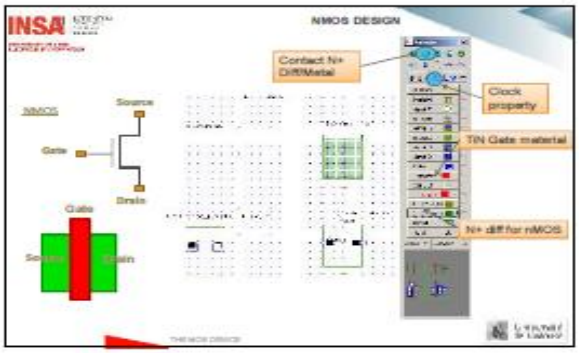
MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

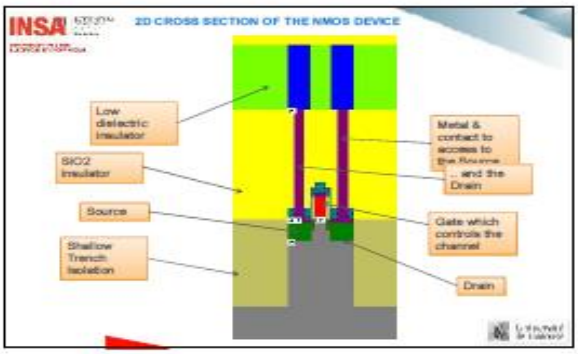
(Autonomous Institution – UGC, Govt. of India)

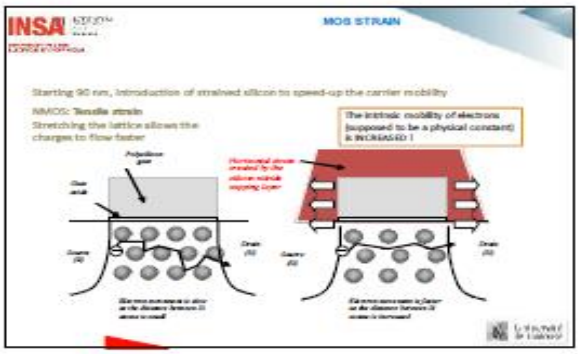
DEPARTMENT OF ECE

CMOS Analog Integrated Circuit Design

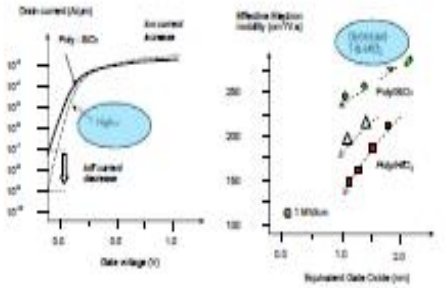
Hand outs-Unit1-5







METAL GATE – STARTING 65NM

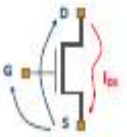


Highest mobility is obtained with optimized TiN/HfO_2

MOS MODEL

A MOS model is

- Made of equations describing IDS(VDS) and IDS(VGS)
- Based on parameters linked with the technology and given by the foundry



If V_{GS}<VTO, the device is in cut-off mode

$$Ids = 0$$

If $V_{GS}-V_{TO}$>VTO, the device is in linear mode

$$Ids = KP\frac{W}{L}\left((V_{GS}-VTO)V_{DS} - \alpha\frac{V_{DS}^2}{2}\right)(1+\lambda V_{DS})$$

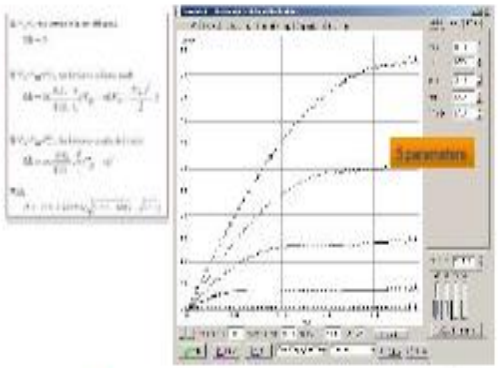
If $V_{GS}-V_{TO}$>VDS, the device is in saturated mode

$$Ids = KP\frac{W}{2L}(V_{GS}-VTO)^2(1+\lambda V_{DS})$$

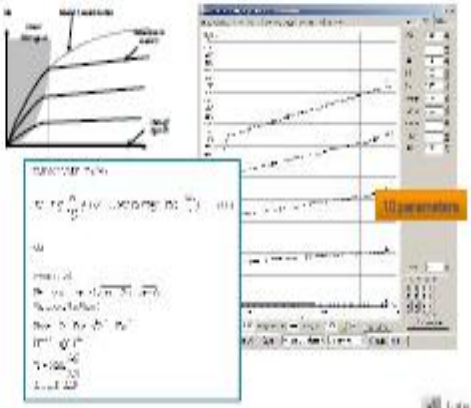
With:

$$VTO = \Phi_{MS} - \frac{Q_{SS}}{C_{ox}} + \gamma\left(\sqrt{|PHI - VBS|} - \sqrt{|PHI|}\right)$$

THE OLD MOS MODEL 1

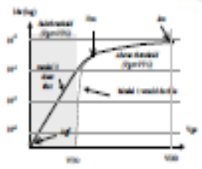


THE MOS MODEL 3

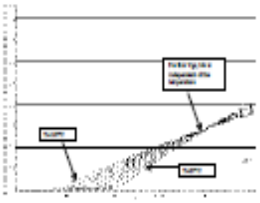


THE MOS MODEL 3

MOS Model 3 takes into account the sub-threshold (VG-VT0) regime

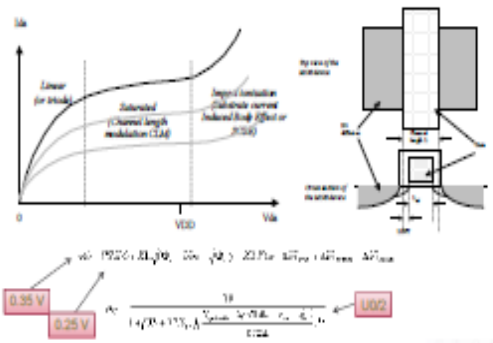


MOS Model 3 takes into account temperature effects



Difference MOS Model 1, Model 3?

THE MOS MODEL BSIM4

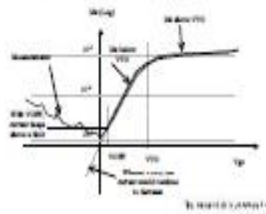


0.35 V

0.25 V

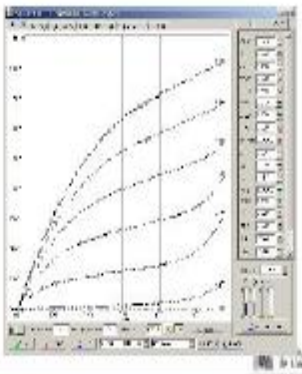
U02

THE MOS MODEL BSIM4

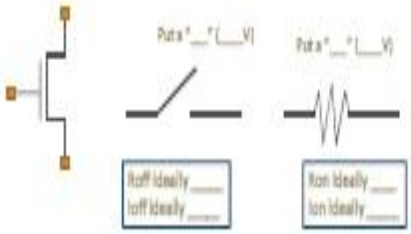


THE MOS MODEL BSIM4

- 20 key parameters listed in Microwind
- Details on BSIM equations in Microwind: Chapter 3 of the book

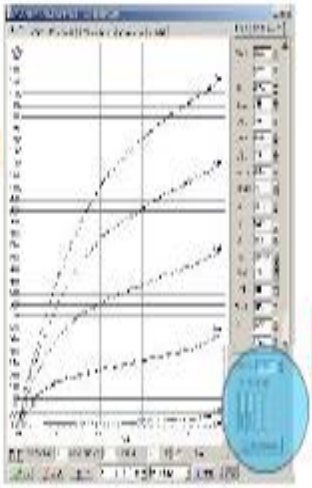


N-CHANNEL MOS AS A SWITCH



N-CHANNEL ION AND RON

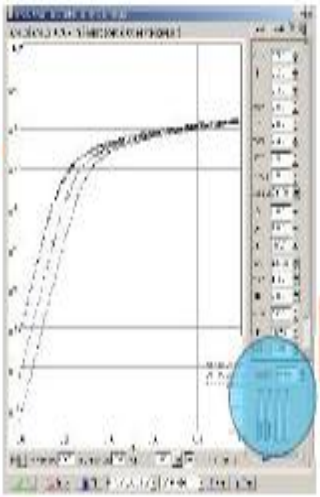
Where is Ron ?



How should I polarize to get Ion ?

N-CHANNEL IOFF AND ROFF

Where is Ioff ?

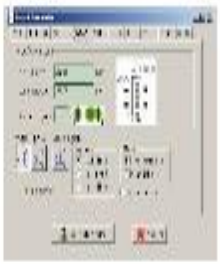


How should I polarize to get Ioff ?

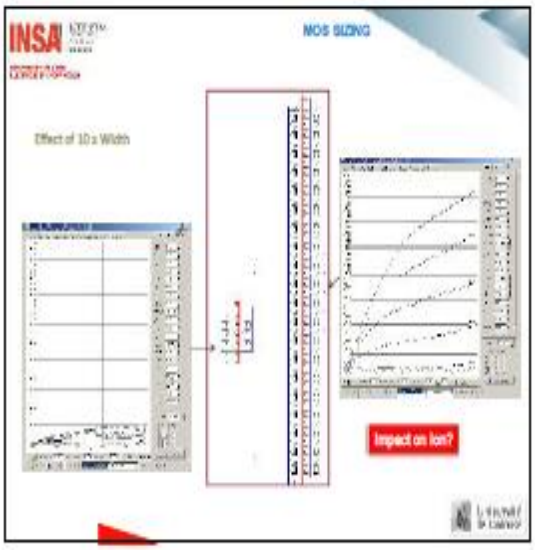
MOS SIZING

If you want to go faster, you can ask for more current

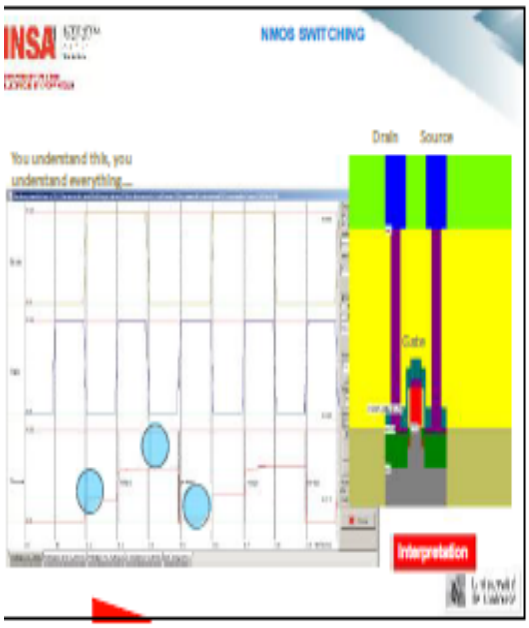
- More current: more W
- You may also reduce L, but by default, L = 2 lambda = Lmin

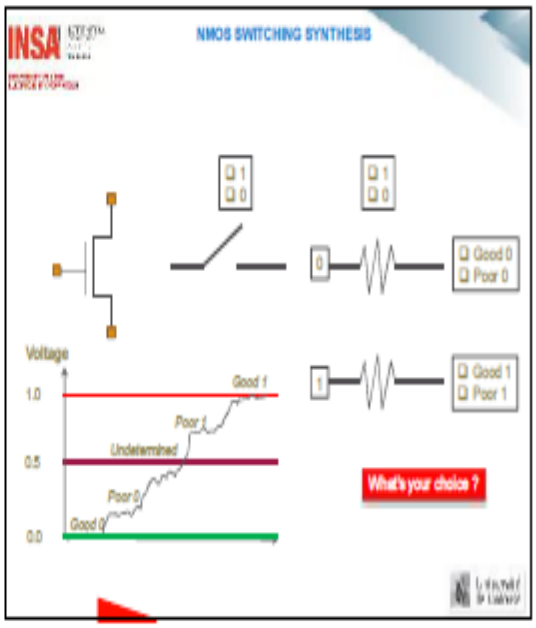


Where is W, L ?

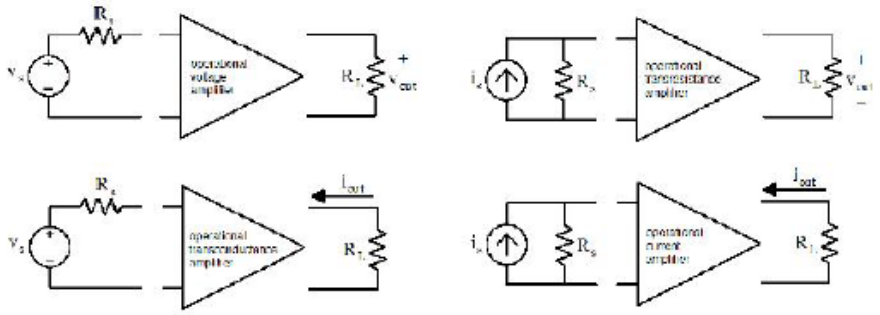

INSA
NOS SIZING
Effect of 10 x Width
Impact on Ion?


INSA
ADD PROPERTIES FOR SIMULATION
At each new Clock, the period increased by 2
"Visible" (eye) is added to view the Source node


INSA
NMOS SWITCHING
You understand this, you understand everything...
Drain
Source
Gate
Interpretation


INSA
NMOS SWITCHING SYNTHESIS
Good 0
Poor 0
Good 1
Poor 1
Voltage
1.0
0.5
0.0
Good 1
Poor 1
Undetermined
Poor 0
Good 0
What's your choice ?

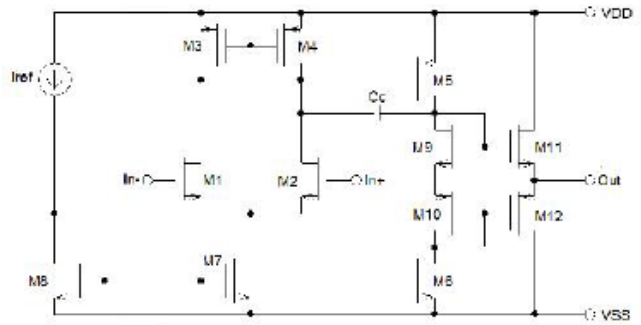
Operational amplifiers



Operational amplifiers are the most widely used block in the analog circuit design. Depending on the mode of representation of the signals (by current or voltage) four broad type of operational amplifiers are known:

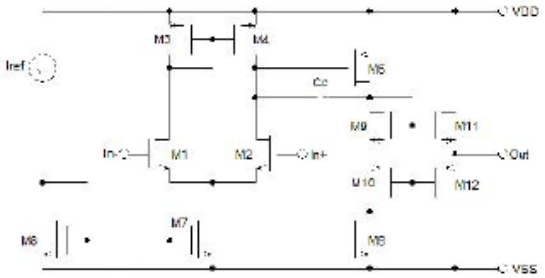
- operational voltage amplifier (usually called Op Amp): voltage input – voltage output;
- operational transconductance amplifier (OTA): voltage input – current output;
- operational transresistance amplifier (current mode amplifier, CMA): current input – voltage output;
- operational current amplifier (OCA): current input – current output.

Basic CMOS Operational Amplifier



The basic CMOS Op Amp configuration consists of two stages. The first stage is a differential amplifier (M1, M2, M7) with current mirror load (M3, M4). It ensures high value of the CMRR. The second stage is a class AB output amplifier with a complementary source-followers (M11,M12). M5 and M6 are common source amplifier with active load. Transistors M9 and M10 set the biasing of the output pair. The couples M8, M7 and M8,M6 are simple current mirrors. Iref is a constant current reference. As we know from previous modules, transistors M1 and M2, and M3 and M4 are identical. Miller capacitance Cc is the frequency compensation of the circuit.

Basic DC relations in the Op Amp



To obtain the basic DC relations in the Op Amp, the circuit is analyzed without exciting signal, i.e.

$V(In+) = V(In-) = 0V$.

Thus

$$I_{ref} = I_{D8} = \frac{\mu_n C_{ox}}{2}\frac{W8}{L8}V_{eff8};$$

$$I_{D7} = \frac{W7/L7}{W8/L8}I_{D8} = \frac{W7/L7}{W8/L8}I_{ref};$$

Because of the symmetry in the input pair

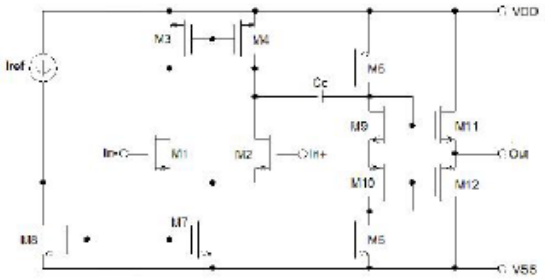
$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D7}}{2} \Rightarrow \mu_n C_{ox}\frac{W1}{L1}V_{eff1} = \mu_p C_{ox}\frac{W3}{L3}V_{eff3}$$

To ensure the symmetrical load of the input diff amp, the next equations should be fulfilled

$$|V_{DS4}| = |V_{DS3}| = |V_{GS5}| \Rightarrow I_{D5} = I_{D3}\frac{W5/L5}{W3/L3} = \frac{I_{D7}}{2}\frac{W5/L5}{W3/L3} = \frac{I_{ref}}{2}\frac{W5/L5}{W3/L3}\frac{W7/L7}{W8/L8}.$$

(continue to the next slide)

Basic DC relations in the Op Amp (cont.)



Using the basic property of the current mirror we can find

$$I_{D6} = I_{ref}\frac{W6/L6}{W8/L8}.$$

Because of currents ID5 and ID6 are equals

$$I_{D5} = I_{D6} = I_{D9} = I_{D10};$$

$$\frac{I_{ref}}{2}\frac{W5/L5}{W3/L3}\frac{W7/L7}{W8/L8} = I_{ref}\frac{W6/L6}{W8/L8}$$

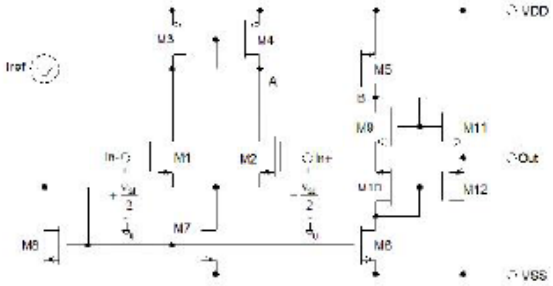
and finally $\frac{W5}{L5}\frac{W7}{L7} = 2\frac{W6}{L6}\frac{W3}{L3}$, which is the condition for normally operation of the circuit.

To assure the desired biasing of the output pair, the transistors M9 and M10 should be sized using the following formulas

$$\frac{L9}{W9} = \frac{2\cdot I_{D5}}{\mu_n C_{ox} V_{eff9}^2}; \quad \frac{L10}{W10} = \frac{2\cdot I_{D5}}{\mu_p C_{ox} V_{eff10}^2};$$

$$I_{D11} = I_{D12} = I_{D6}\frac{W12/L12}{W10/L10} = I_{D6}\frac{W11/L11}{W9/L9}.$$

Low-frequency analysis of Op Amp



The formulas for voltage gain **Au** and output resistance r_{out} of the OP Amp can be obtained by using the equations for the simple amplifying stages, given in Module 3. Hence, the signals at point A and B are as follow

$$v_A = A_{u1} v_{id} = \frac{g_{m2}}{g_{o2} + g_{o4}} v_{id} \text{ and}$$

$$v_B = A_{u2} v_A = \frac{-g_{m5}}{g_{o5} + g_{o6}} v_A$$

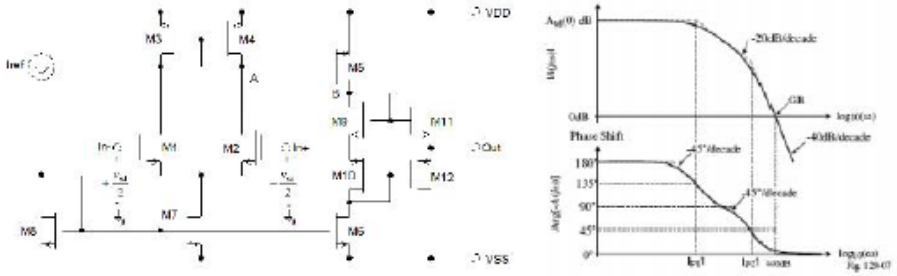
The final results are $A_u = A_{u1} A_{u2} = \frac{v_{out}}{v_{id}} \approx \frac{v_B}{v_{id}} = \frac{-g_{m2}\, g_{m5}}{(g_{o2} + g_{o4})(g_{o5} + g_{o6})}$ and $r_{out} = \frac{1}{g_{m11} + g_{m12}}$,

where

$$g_{m2} = \sqrt{2\mu_n C_{ox} \frac{W2}{L2} I_{d2}} = \mu_n C_{ox} V_{eff2} = \frac{2I_{D2}}{V_{eff2}}; \quad g_{m5} = \sqrt{2\mu_p C_{ox} \frac{W5}{L5} I_{d5}} = \mu_p C_{ox} V_{eff5} = \frac{2I_{D5}}{V_{eff5}}$$

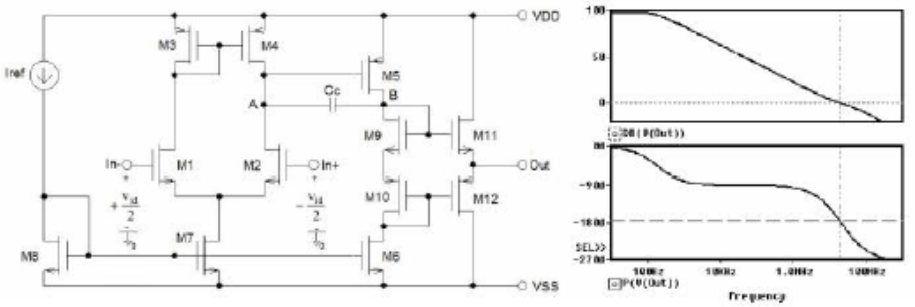
$$g_{o2} = \lambda_{n2} I_{D2}; \quad g_{o4} = \lambda_{p4} I_{D2}; \quad g_{o5} = \lambda_{p5} I_{D5}; \quad g_{o6} = \lambda_{n6} I_{D5}.$$

High-frequency behavior of Op Amp



The discussed circuit has the disadvantage of having two high-impedance nodes in points A and B. This implies that two poles will be dominant, which deteriorate the phase margin of the Op Amp. The right graphic shows the open loop uncompensated frequency response of the amplifier. There are two poles in the circuit and at the point at which the open-loop gain is unity (0 dB) corresponds the phase shift is higher than 180 degree. As we know the maximum admissible phase shift is 135 degree, which assures a phase margin of 45 degree. Otherwise the circuit is highly unstable, as it is in our case. To avoid the instability the frequency compensation is used, which guarantees a phase margin no less than a 45 degree. (Frequently, 60 degree is desired for better safety).

Frequency compensation of Op Amp



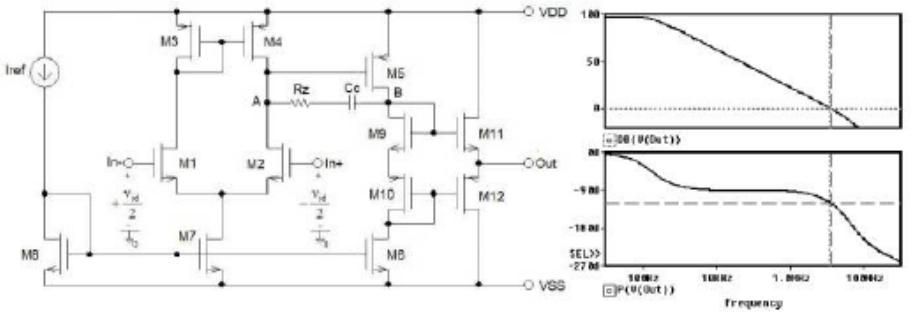
To compensate the Op Amp the capacitor **Cc** is used. In this way the dominant pole is translated towards the low frequencies. The next formula can be used for calculation the value of the capacitor **Cc**.

$$f_u \approx GBW = A_u BW \approx A_{u1}A_{u2}\frac{g_{02}+g_{o4}}{2\pi A_{u2}C_c} = A_{u1}\frac{g_{02}+g_{o4}}{2\pi C_c} = \frac{g_{m2}}{g_{o2}+g_{o4}}\frac{g_{02}+g_{o4}}{2\pi C_c} = \frac{g_{m2}}{2\pi C_c}$$

In this formula, **fu** is the frequency, at which the open-loop gain is unity (usually is known as unity-gain frequency). The value of **fu** is very close to the gain-bandwidth product, **GBW**.

But the results shown in the right graphics demonstrate that despite of applied compensation the Op Amp is unstable again. An additional right-hand plane zero appears, which boosts the magnitude while decreasing the phase.

Zero compensation of Op Amp

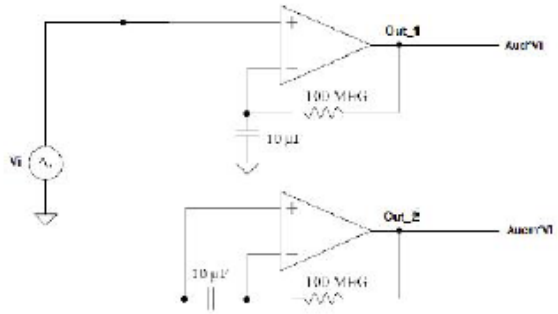


As we seen in the previous slide, when the compensation capacitor is included, the right-hand plane zero appears. Its value is given by $z = g_{m5}/C_c$. To eliminate the problem a resistor in series with the compensation capacitor can be included. Then the formula for zero changes

$$z = \left[C_c\left(\frac{1}{g_{m5}} - R_z\right)\right]^{-1}.$$

If **Rz** is selected equal to $1/g_{m5}$ the zero disappears. If **Rz** is larger than $1/g_{m5}$ the phase margin increases. In the discussed case the result is extremely positive. The using of zero nulling resistor increases the phase margin up to 60 degree.

Common mode rejection ratio

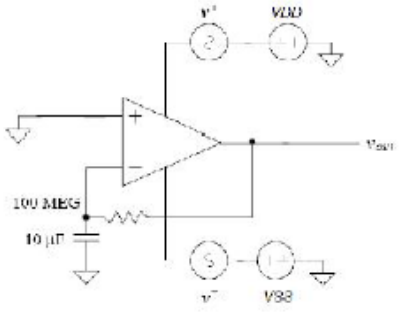


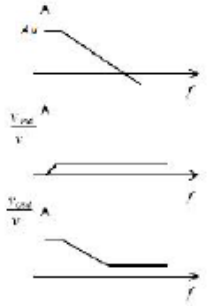
Common-mode rejection ratio, **CMRR**, is defined as the ratio of the differential voltage amplification **Aud** to the common-mode voltage amplification **Aucm**. Ideally this ratio would be infinite with common mode voltages being totally rejected.

The figure shows the test-circuit for CMRR simulation. The formula for CMRR calculation is

$$\mathrm{CMRR} = 20\log\left(\frac{A_{ud}}{A_{ucm}}\right) = 20\log\left(\frac{V(\mathrm{Out\_1})}{V(\mathrm{Out\_2})}\right).$$

Power supply rejection ratio



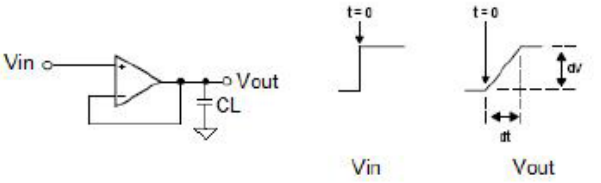


The power supply rejection ratio, **PSRR**, describes how well an amplifier rejects noise or changes on the VDD and VSS power supply. The figure shows the test-circuit for PSRR simulation. The formulas for PSRR calculation are

$$\mathrm{PSRR}^{+} = \frac{\mathrm{Au}}{v_{out}/v^{+}}; \quad \mathrm{PSRR}^{-} = \frac{\mathrm{Au}}{v_{out}/v^{-}}.$$

The right plots demonstrate the frequency characteristics of the three components of the above formulas.

Slew rate

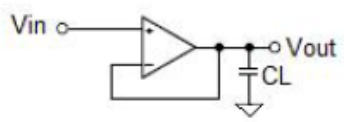


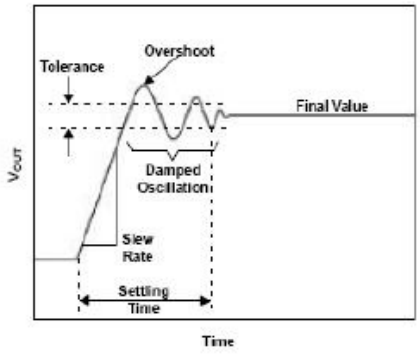
$$SR = \frac{dVout}{dt}$$

$$BOM = \frac{SR}{2\pi Vo\,min}$$

Slew rate, **SR**, is the rate of change in the output voltage caused by a step input. Its units are V/μs or V/ms. Figure shows slew rate graphically. The primary factor controlling slew rate in most op amps is the internal compensation capacitor Cc, which is added to make the op amp unity gain stable. In op amps without internal compensation capacitors, the slew rate is determined by the load capacitor CL. The slew rate is limiting factor for Maximum output-swing bandwidth, **BOM**. As the frequency gets higher and higher the output becomes slew rate limited and can not respond quickly enough to maintain the specified output voltage swing. BOM specifies the bandwidth over which the output is above a specified value Vomin.

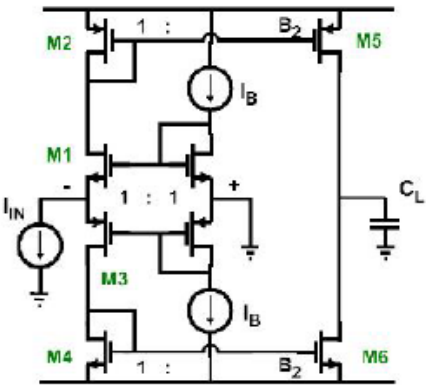
Settling time





The settling time characterizes the finite time for a signal to propagate through the internal circuitry of an op amp. In fact it takes a period of time for the output to react to a step change in the input. In addition, the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Settling time, ts, is the time required for the output voltage to settle to within a specified percentage of the final value given a step input. Figure shows this graphically. Settling time is a design issue in data acquisition circuits when signals are changing rapidly.

Operational current amplifier

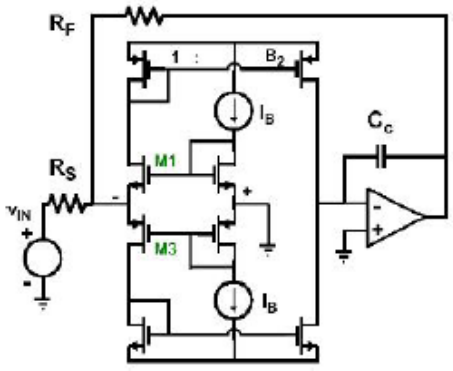


$$A_R = B_2 r_{out} = \frac{B_2}{g_{o5} + g_{06}}; \quad BW = \frac{1}{2\pi C_L r_{out}};$$

$$A_R BW = \frac{B_2}{2\pi C_L}; \quad SR = B_2 \frac{I_{in}}{C_L}$$

The Operational current amplifiers **OCA** uses of input common-gate stages M1 and M3, which are biased at current I_B. The signals from the drains of M1 and M3 are current mirrored to the output, with current factor B_2. For small-signals, the input current i_{IN} is divided over both input transistors, multiplied by B_2, and generates an output voltage in the output resistance r_{out}. The current gain is very modest (B_2) but the transresistance (A_R) can be very large. It is not possible to compare the product $A_R BW$ to the **GBW** of a voltage amplifier. They have totally different dimensions. The main advantage of this amplifier is that the Slew Rate is unlimited. Indeed, for a large input current, the SR is determined by this input current itself, multiplied by B_2.

Operational current mode amplifier

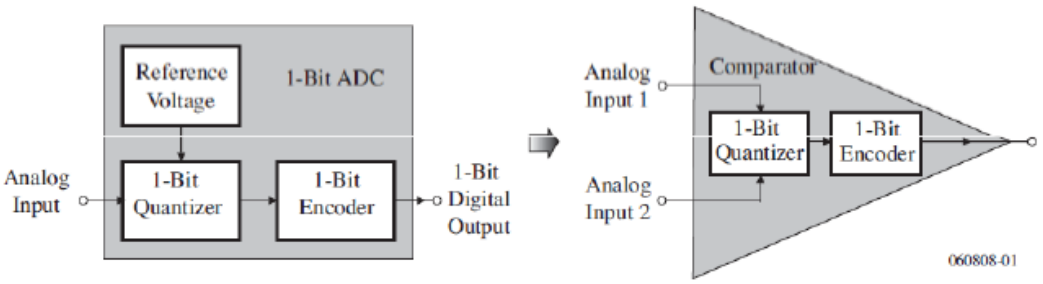


The presented two-stage opamp has a OCA as a input stage and standard voltage-to-voltage stage as a second stage. Such operational amplifiers are known as Operational current-mode amplifiers CMA. In this circuit the low-voltage gain A_{u0} is defined from R_F/R_S ratio, as in voltage-to-voltage Op Amps. However, due to the current feedback, the expressions for the bandwidth are now different. The **BW** is determined by the feedback resistor R_F, while the series resistor R_S controls the **GBW**.

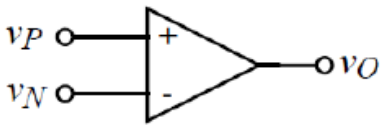
$$A_u = -\frac{R_F}{R_S}\frac{1}{1 + j\omega R_F C_C}; \quad A_{u0} = -\frac{R_F}{R_S}; \quad BW = \frac{1}{2\pi R_F C_C}; \quad GBW = |A_{u0}| \cdot BW = \frac{1}{2\pi R_S C_C}$$

Comparator

- ✓ The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison.
- ✓ The comparator is basically a 1-bit analog-to-digital converter

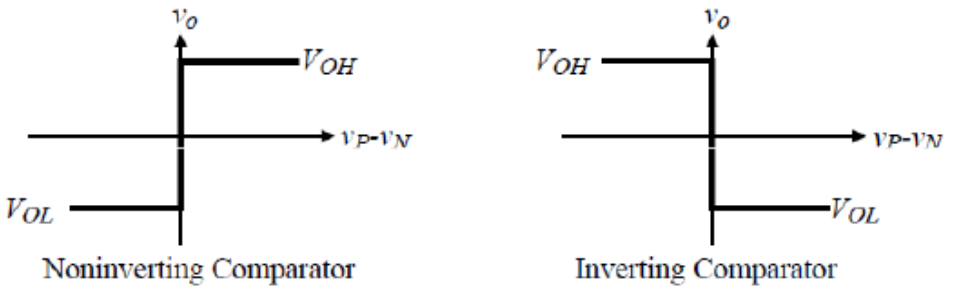


- ✓ Comparator symbol



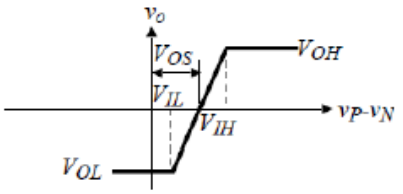
Non-inverting and Inverting Comparators

- ✓ The comparator output is binary with the two-level outputs defined as,
  - VOH = the high output of the comparator
  - VOL = the low level output of the comparator
- ✓ Voltage transfer function of a Non-inverting and Inverting Comparator



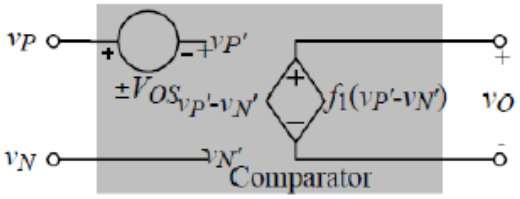
Input Offset Voltage of a Comparator

- ✓ Voltage transfer curve



V_{OS} = the input voltage necessary to make the output equal $\frac{V_{OH}+V_{OL}}{2}$ when $v_P = v_N$.

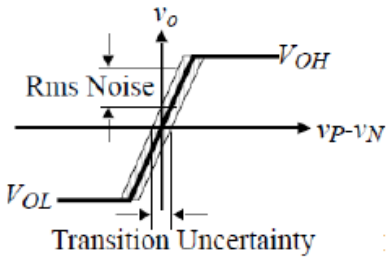
- ✓ Model



- ✓ Other aspects of the model:
  - ICMR = input common mode voltage range (all transistors remain in saturation)
  - Rin = input differential resistance
  - Ricm = common mode input resistance

Comparator Noise

- ✓ Noise of a comparator is modeled as if the comparator were biased in the transition region



- ✓ Noise leads to an uncertainty in the transition region causing jitter or phase noise

Input Common Mode Range

- ✓ Because the input is analog and normally differential, the input common mode range of the comparator is also important
- ✓ Input common mode range (*ICMR):*
  - ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance
- ✓ The ICMR is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region

Linear Frequency Response – Dominant Single-Pole

Model:

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1}$$

where

$A_v(0)$ = dc voltage gain of the comparator

$\omega_c = \frac{1}{\tau_c}$ = -3dB frequency of the comparator or the magnitude of the pole

Step Response:

$$v_o(t) = A_v(0)\,[1 - e^{-t/\tau_c}]V_{in}$$

where

V_{in} = the magnitude of the step input.

Maximum slope of the step response:

$$\frac{dv_o(t)}{dt} = \frac{A_v(0)}{\tau_c} e^{-t/\tau_c} V_{in}$$

The maximum slope occurs at $t = 0$ giving,

$$\frac{dv_o(t)}{dt}\Big|_{t=0} = \frac{A_v(0)}{\tau_c} V_{in}$$

Dynamic Characterization – Slew Rate

- ✓ If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by the slew rate
- ✓ Slew rate comes from the relationship $i = C\frac{dv}{dt}$
  - where i is the current through a capacitor and v is the voltage across it
- ✓ If the current becomes limited, then the voltage rate becomes limited, Therefore for a comparator that is slew rate limited, then

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 \cdot SR}$$

- ✓ where
  - SR = slew rate of the comparator
  - If SR < |maximum slope|, then the comparator is slewing

Example - Propagation Delay Time of a Comparator

Find the propagation delay time of an open loop comparator that has a dominant pole at 10^3 radians/sec, a dc gain of 10^4, a slew rate of 1V/μs, and a binary output voltage swing of 1V. Assume the applied input voltage is 10mV.

Solution

The input resolution for this comparator is 1V/10^4 or 0.1mV. Therefore, the 10mV input is 100 times larger than v_{in}(min) giving a k of 100. Therefore, we get

$$t_p = \frac{1}{10^3} ln\left(\frac{2 \cdot 100}{2 \cdot 100 - 1}\right) = 10^{-3}\, ln\left(\frac{200}{199}\right) = 5.01\mu s$$

For slew rate considerations, we get

$$\text{Maximum slope} = \frac{10^4}{10^{-3}} \cdot 10\text{mV} = 10^5 \text{ V/sec.} = 0.1\text{V}/\mu\text{s}.$$

Therefore, the propagation delay time for this case is limited by the linear response and is 5.01μs.

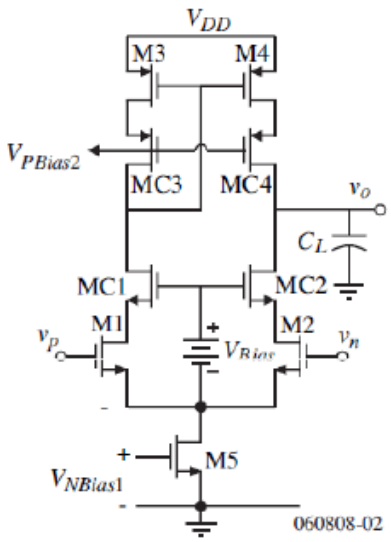
Open-loop Comparators

SINGLE-POLE COMPARATORS

Dominant Pole Comparators

- ✓ Any of the self-compensated op amps provide a straight-forward implementation of an open loop comparator without any modification.
- ✓ The previous section give the relationships for:
  - – The static characteristics
    - Gain
    - Input offset
    - Noise
  - – The dynamic characteristics
    - Linear frequency response
    - Slew rate response

Single-Stage Dominant Pole Comparator



- Gain $\approx g_m^2 r_{ds}^2$
- Slew rate = I_5/C_L
- Dominant pole = $-1/(R_{out}C_L) = -1/(g_m r_{ds}^2 C_L)$

Example - Performance of a Two-Stage Comparator

Evaluate V_{OH}, V_{OL}, $A_v(0)$, $V_{in}(\min)$, p_1, p_2, for the two-stage comparator Assume that this comparator is the circuit of op amp with no compensation capacitor, C_c, and the minimum value of $V_{G6} = 0$V. Also, assume that $C_I = 0.2$pF and $C_{II} = 5$pF.

Solution

Using the above relations, we find that

$$V_{OH} = 2.5 - (2.5\text{-}0\text{-}0.7)\left[1 - \sqrt{1 - \frac{8{\cdot}234\text{x}10^{-6}}{50\text{x}10^{-6}{\cdot}38(2.5\text{-}0\text{-}0.7)^2}}\right] = 2.2\text{V}$$

The value of V_{OL} is -2.5V. The gain was evaluated in Ex. 6.3-1 as $A_v(0) = 7696$. Therefore, the input resolution is

$$V_{in}(\min) = \frac{V_{OH}\text{-}V_{OL}}{A_v(0)} = \frac{4.7\text{V}}{7696} = 0.611\text{mV}$$

Next, we find the poles of the comparator, p_1 and p_2. From Ex. 6.3-1 we find that

$$p_1 = -\frac{g_{ds2} + g_{ds4}}{C_I} = -\frac{15\text{x}10^{-6}(0.04+0.05)}{0.2\text{x}10^{-12}} = -6.75\text{x}10^6\ (1.074\text{MHz})$$

and

$$p2 = -\frac{g_{ds6} + g_{ds7}}{C_{II}} = -\frac{95\text{x}10^{-6}(0.04+0.05)}{5\text{x}10^{-12}} = -1.71\text{x}10^6\ (0.272\text{MHz})$$

Step Response of a Two-Stage Comparator

- ✓ Find the maximum slope of Two stage comparator and the time it occurs if the magnitude of the input step is vin(min). If the dc bias current in M7 is 100μA, at what value of load capacitance, CL would the transient response become slew limited? If the magnitude of the input step is 100vin(min), what is the new value of CL at which slewing would occur?

Solution

- ✓ The poles of the comparator were given as p_1 = -6.75x106 rads/sec p_2 = -1.71x106 rads/sec. This gives a value of m = 0.253. From the previous expressions, the maximum slope occurs at $t_n(\max)$ = 1.84 secs. Dividing by |p1| gives t(max) = 0.272μs. The slope of the transient response at this time is found as

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = -0.338[\exp(-1.84) - \exp(-0.253{\cdot}1.84)] = 0.159\ \text{V/sec}$$

Multiplying the above by $|p_1|$ gives $\frac{dv_{out}'(t(\max))}{dt} = 1.072\text{V}/\mu\text{s}$

If the slew rate is less than $1.072\text{V}/\mu\text{s}$, the transient response will experience slewing. Therefore, if $C_L \geq 100\mu\text{A}/1.072\text{V}/\mu\text{s}$ or 93.3pF, the comparator will slew.

If the input is $100v_{in}(\min)$, then we must unnormalize the output slope as follows.

$$\frac{dv_{out}'(t(\max))}{dt} = \frac{v_{in}}{v_{in}(\min)}\frac{dv_{out}'(t(\max))}{dt} = 100{\cdot}1.072\text{V}/\mu\text{s} = 107.2\text{V}/\mu\text{s}$$

Therefore, the comparator will now slew with a load capacitance of 0.933pF.

Summary

- ✓ The two-stage, open-loop comparator has two poles which should as large as possible
- ✓ The transient response of a two-stage, open-loop comparator will be limited by either the bandwidth or the slew rate
- ✓ It is important to know the initial states of a two-stage, open-loop comparator when finding the propagation delay time
- ✓ If the comparator is gain bandwidth limited then the poles should be as large as possible for minimum propagation delay time
- ✓ If the comparator is slew rate limited, then the current sinking and sourcing ability should be as large as possible

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.TECH (VLSI &ES) (2019-21 Batch)

ROLL LIST

S.NO	HALL TICKET NUMBER	NAME OF THE STUDENT
1	19N31D6801	ADEPU HARI PRIYA
2	19N31D6802	ALGAPALLY SANTOSH SAGAR
3	19N31D6803	BADDAM SINDHU REDDY
4	19N31D6804	BANGARIGALLA SHEKARBABU
5	19N31D6805	CHIPPA PRITHVIRAJ
6	19N31D6806	DANAVATH NAGAMMA
7	19N31D6807	DEETI ADIKYA
8	19N31D6808	DOKKU VARA LAKSHMI
9	19N31D6809	GADHARI KEERTHANA
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11	19N31D6811	KATTA VIDUSHEE KUMARI VISHWA KARMA
12	19N31D6812	KODE SASIKALA
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14	19N31D6814	NAGANABOINA SUMAN
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16	19N31D6816	POLAPALLI SRIKANTH
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24	19N31D6824	VUTUKURI ANUSHA

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Internal Exam Evaluation

S.NO	HALL TICKET NO	MID-I	MID-II	AVERAGE
1	19N31D6801	26	12	19
2	19N31D6802	27	26	26.5
3	19N31D6803	12	26	19
4	19N31D6804	12	21	16.5
5	19N31D6805	21	26	23.5
6	19N31D6806	26	26	26
7	19N31D6807	26	22	24
8	19N31D6808	26	25	25.5
9	19N31D6809	26	26	26
10	19N31D6810	26	24	25
11	19N31D6811	25	25	25
12	19N31D6812	29	26	27.5
13	19N31D6813	27	24	25.5
14	19N31D6814	24	21	22.5
15	19N31D6815	20	22	21
16	19N31D6816	26	26	26
17	19N31D6817	24	18	21
18	19N31D6818	24	20	22
19	19N31D6819	20	19	19.5
20	19N31D6820	28	27	27.5
21	19N31D6821	19	22	20.5
22	19N31D6822	12	23	17.5
23	19N31D6823	21	12	16.5
24	19N31D6824	21	20	20.5

End/Mid Questions

UNIT-I
MOS DEVICES AND MODELING

1.Discuss about the Passive Components of the MOS transistor.
2.Explain about the CMOS device Modeling.
3.Explain the Large-signal model for the MOS Transistor.
4.Draw the small-signal model for the MOS transistor. Briefly explain each component
5.Explain about the computer simulation models.

UNIT-II ANALOG CMOS SUB CIRCUITS

1. Write short notes on current sinks and sources.
2. What is Current Mirror? Explain the general properties of current mirrors with block diagram.
3. Explain the cascode current mirror and Wilson current mirror using bipolar and MOS devices.
4. Explain the following:
   i) Simplest form of Current Mirror in Bipolar and MOS
   ii) Simplest form of Current Mirror with beta helper in Bipolar and MOS
   iii) Simplest form of Current Mirror with degeneration in Bipolar and MOS

UNIT III CMOS AMPLIFIERS

1. Draw and explain the small signal frequency response of the active resistor load inverter.
2. Briefly explain the differential amplifiers. With necessary equation give the large signal analysis of CMOS differential amplifiers.
3. Explain the large signal characteristics of cascode amplifier.
4. What is a current amplifier? Explain the single ended input current amplifier.
5. Write short notes on Output amplifiers.
6. Explain about high gain amplifier architectures.

UNIT IV CMOS OPERATIONAL AMPLIFIERS

1. Explain about the design of CMOS op-amps.
2. Explain about the two stage operational amplifier analysis.
3. Derive the expression for power-supply rejection ratio of Two-stage op-amps.
4. What is compensation of op amp? Explain the operation of Miller compensation.
5. Explain about the Cascode Op-amps.
6. Explain the Measurement technologies of Op-amp.

UNIT V COMPARATORS

1. What are the characterizations of comparators? Calculate the gain and propagation delay of two stage comparator.
2. Draw and explain the two stage open loop comparator.
3. Explain the types of discrete time comparator circuit.(or)
4. Explain the following terms with neat sketch.
   a) Switched capacitor comparators
   b) Regenerative comparators
5. How to improve the performance of open loop comparators? Explain it.

R15

Code No: R15D6805

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

CMOS Analog Integrated Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

*****

SECTION-I

1 **(a)** Explain about MOS large- signal analysis of CMOS Device Modeling **[10M]**
(b) Explain sub-threshold MOS model Parameters. **[5M]**

OR

2 **(a)** Discuss about the passive components of the MOS transistor. **[7M]**
(b) Write about computer simulation models for MOS transistor **[8M]**

SECTION-II

3 a) Explain the working of current mirror with beta helper **[10M]**
b) Explain the operation of MOS Diode **[5M]**

OR

4 Discuss the Cascode current Mirror and Wilson Current Mirror **[15M]**

SECTION-III

5 (a)Explain about working of differential amplifier **[10M]**

(b)Explain the operation of CMOS inverter **[5M]**

OR

6	Discuss the principle of High Gain Amplifiers Architectures	**[15M]**

SECTION-IV

7	Discuss the concept of op amp compensation and give the necessary expressions.	**[15M]**

OR

8	(a)Explain the Design of Two-Stage Op Amps	**[10M]**
	(b)What are the various measurements of op amp?	**[5M]**

SECTION-V

9	(a) Explain the Discrete-Time Comparators.	**[7M]**
	(b) What is a comparator and list the important characteristics of a comparator	**[8M]**

OR

10	What are the various forms of improving the slew-rate of a 2-stage op amp and obtain the expression for slew rate of CMOS op amp	**[15M]**

****

R17

Code No: **R17D6805**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Regular/Supplementary Examinations, Dec-18/Jan 19

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

SECTION-I

Q.No. 1.a. Draw the physical structure of n channel and p channel MOS transistor using well technology and highlight the importance points? [7M]

b. Explain the importance of BSIM3 model addresses threshold voltage reduction? [7M]

OR

Q.No 2.a. Explain the small signal model for the MOS transistor? [7M]

b. Explain about CMOS device model? [7M]

SECTION-II

Q.No.3.a. Explain the the feedback through effects by using a dummy transistor? [7M]

b.Draw the current sink circuits and explain the VI characteristics? [7M]

OR

Q.No.4.a. What do you mean by band gap reference and list the principle involved? [7M]

b.Draw the circuit diagram of standard cascode current sink and how its reduces the errors in V or I? [7M]

SECTION-III

Q.No.5.a. Draw the circuit diagram of output amplifier using push pull inverting amplifier and comment on it? [7M]

b. Explain the noise model of a p channel differential amplifier ? [7M]

OR

Q.No.6.a. Explain the design relationships for the differential amplifier? [7M]

b. Draw the circuit diagram of differential mode and common mode circuits using CMOS and explain? [7M]

SECTION-IV

Q.No.7. What is compensation of Op-amp? Explain the operation of Miller compensation. [14M]

OR

Q.No.8.a. Explain the design procedure for the 2 stage CMOS opamp? [7M]

b.Explain folded cascode op amp? [7M]

SECTION-V

Q.No.9.a. Explain regenerative comparators? [7M]

b. Draw the switched capacitor comparator and highlight four important points? [7M]

OR

Q.No.10.a. How to improve the performance of an open loop high gain comparator by auto zeroing? [7M]

b. Explain clamped push pull output comparator? [7M]

****